

MODEL NAME : EDP51
EDB51

PCB NO : LA-H331P

BOM P/N :

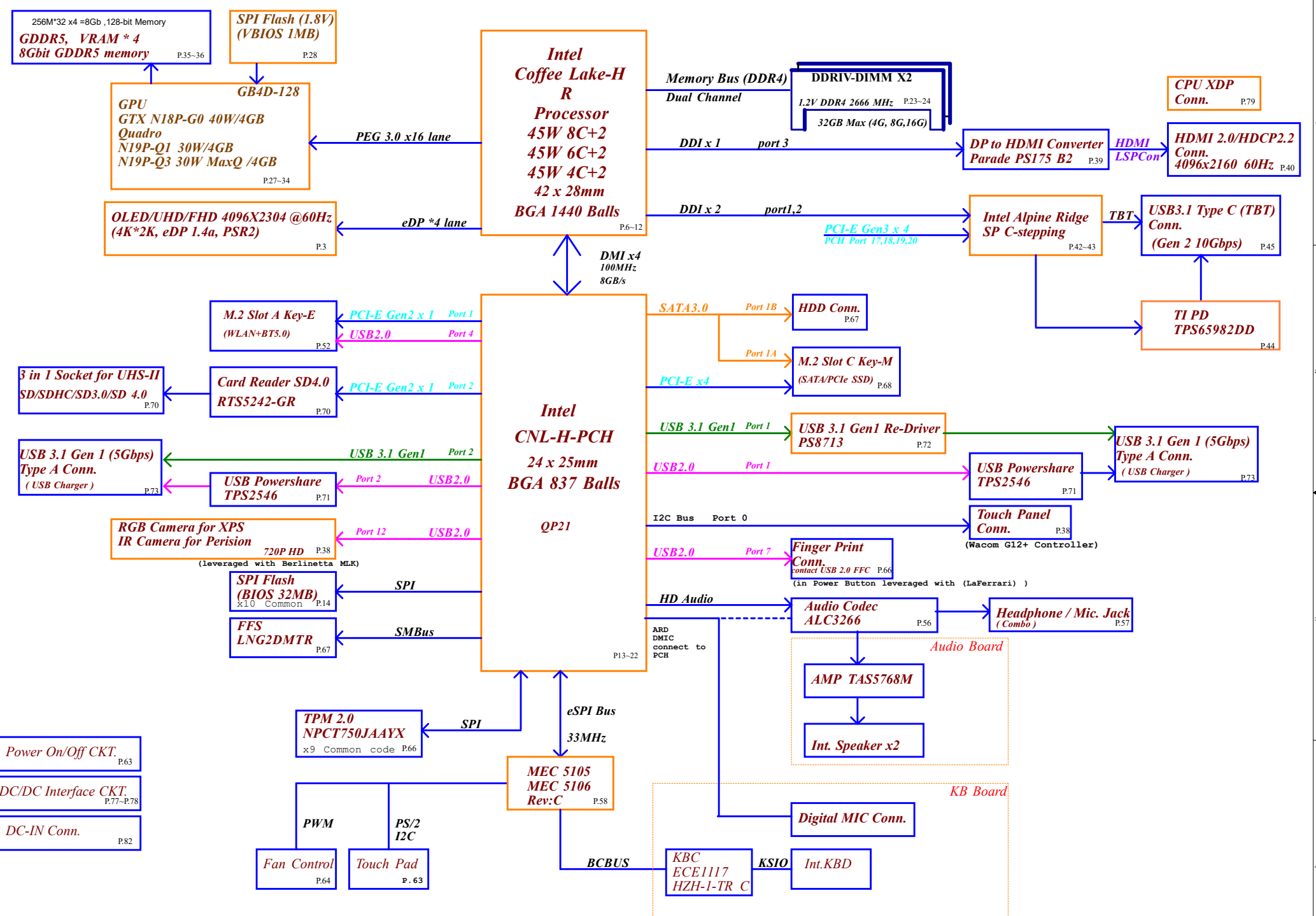
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Schematic Document

Berlinetta CFL R

2019-04-30
Rev: PVT 1.0 (A00)

@	N18PG0@
@EMC@	N19PQ1@
@RTD3@	N19PQ3Q@
CONN@	N18PG0VRAMH@
TP@	N18PG0VRAMM@
3PHASEI5@	N18PVRAMS@
4PHASE62@	N19PQVRAMH@
4PHASE82@	N19PQVRAMM@
EMC@	NVPRO@
IRCAM@	VPRO@
SPAD@	XDP@
UMA@	SRFDM@
DIS@	SRF6X@
5105@	SRFCN@
5106@	SRF6U@
	SRFD1@
	SRFD0@
	SRFCK@
	SRFCZ@



RE67	CE51	REV	PHASE
240K	4700p		PRE EVT
130K	4700p	X00	EVT
62K	4700p	X01	DVT1
33K	4700p	X02	DVT2
8.2K	4700p		
4.3K	4700p		
2K	4700p		
1K	4700p	A00	PVT

USB3.1	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	None
5	None
6	None

USB 2.0	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	NGFF-1 WLAN + BT
5	None
6	None
7	Finger Print
8	None
9	None
10	None
11	None
12	RGB CAMERA

USB OC#	DESTINATION
0	USB Conn 1 (Right Side)
1	USB Conn 2 (Left Side)
2	
3	
4	
5	
6	
7	

PCI EXPRESS	DESTINATION	USB3.0	DESTINATION
Lane 1	NGFF-1 WLAN + BT	7	None
Lane 2	None	8	None
Lane 3	None	9	None
Lane 4	None	10	None
Lane 5	CARD READER		
Lane 6	None		
Lane 7	None		
Lane 8	None		
Lane 9	SSD		
Lane 10	SSD	SATA	DESTINATION
Lane 11	SSD	0A	N/A
Lane 12	SSD	1A	SSD
Lane 13	None	0B	N/A
Lane 14	None	1B	N/A
Lane 15	None	2	HDD
Lane 16	None	3	N/A
Lane 17	Alpine Ridge	4	N/A
Lane 18		5	N/A
Lane 19			
Lane 20			

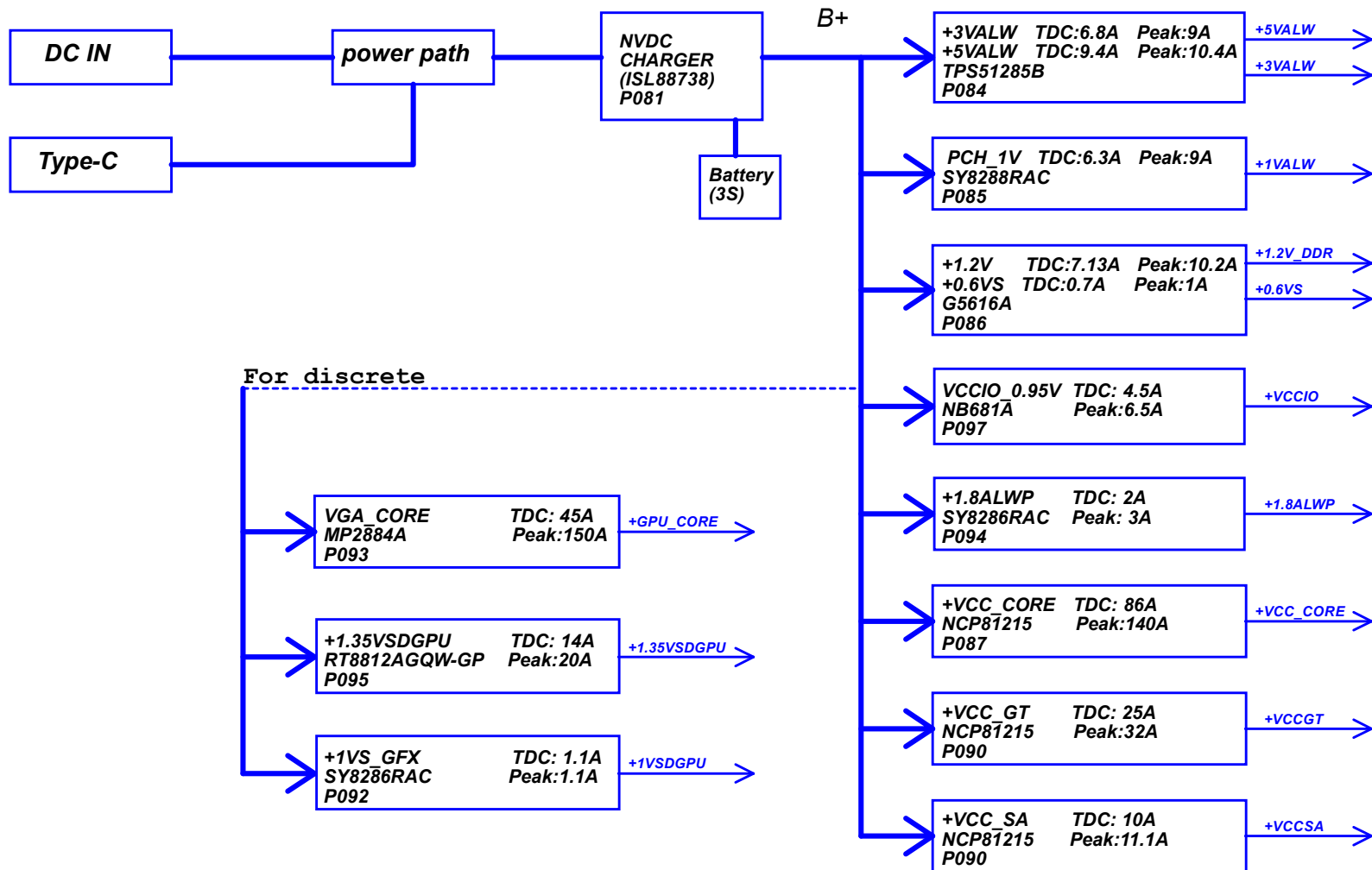
DDI	DESTINATION
1	Alpine Ridge
2	Alpine Ridge
3	HDMI 2.0

LPC	DESTINATION
ESPI/LPC0	MEC5105
LPC1	DEBUG PORT

CLKOUT_PCIE	DESTINATION	CLKOUT_PCIE	DESTINATION
0	None	10	None
1	None	11	None
2	None	12	None
3	NGFF-1 WLAN	13	None
4	CARD READER	14	None
5	Thunderbolt	15	None
6	NGFF-2 SSD		
7	GPU		
8	None		
9	None		

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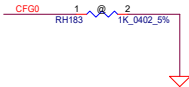
High-Speed I/O [HSIO] Type and Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	PCIe 1.0 Gen2	
Thunderbolt 3/4 Support	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No



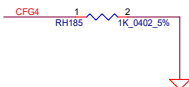
@ : Nopop Component
 @DIS@ : Nopop Component
 DIS@: POP for discrete GPU SKU

CFG Straps for Processor

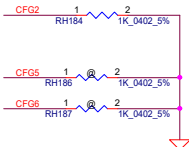
Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	<p>* 1 = (Default) Normal Operation; No stall.</p> <p>0 = Stall.</p>



Display Port Presence Strap	
CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>★ 0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>



PCIe Port Bifurcation Straps	
	*1: (Default) x16 - Device 1 functions 1 and 2 disabled
CFG[6:5]	x0: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
	01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
	00: x8, x4, x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	<p>★ 1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>

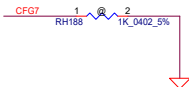
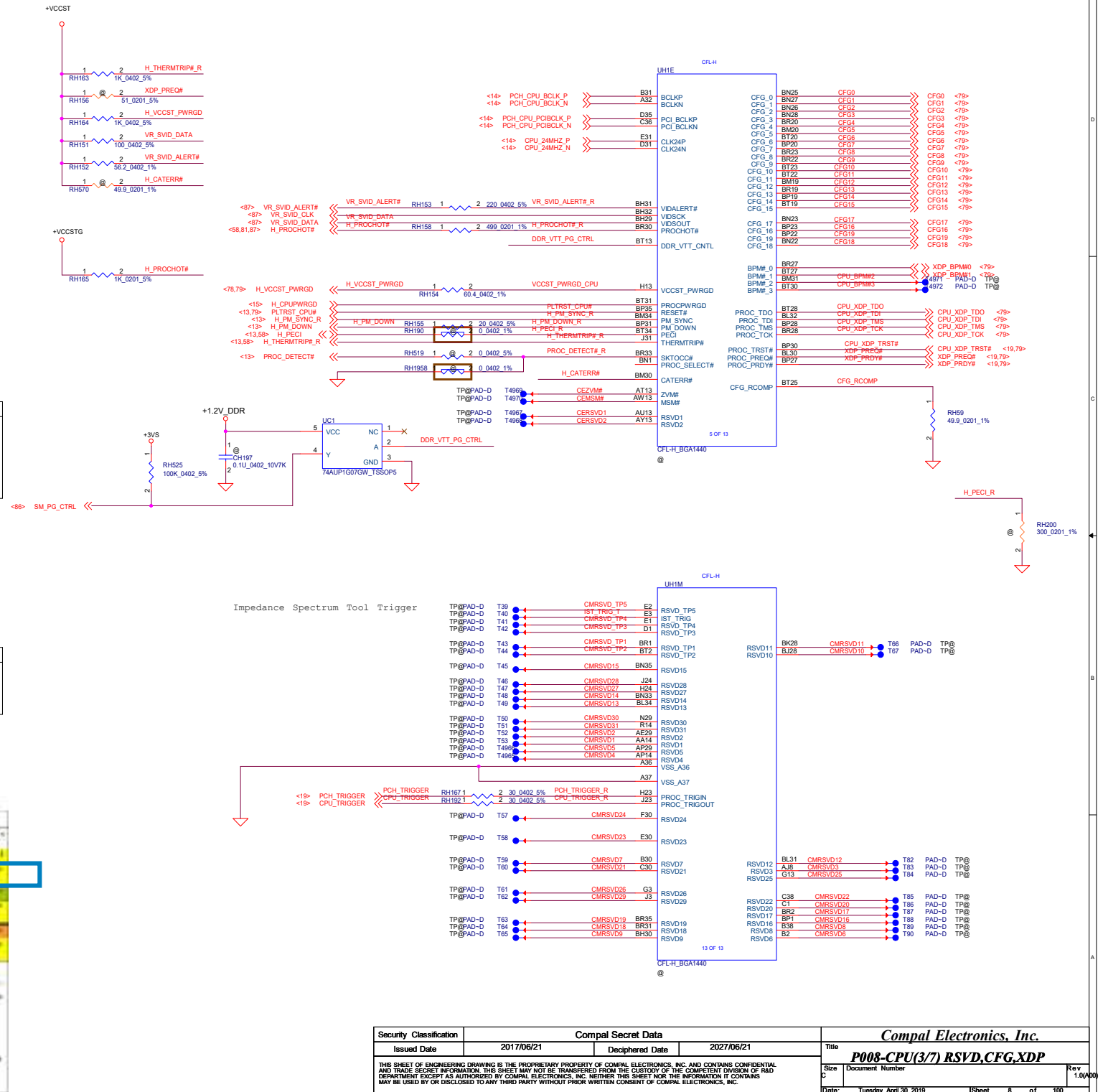
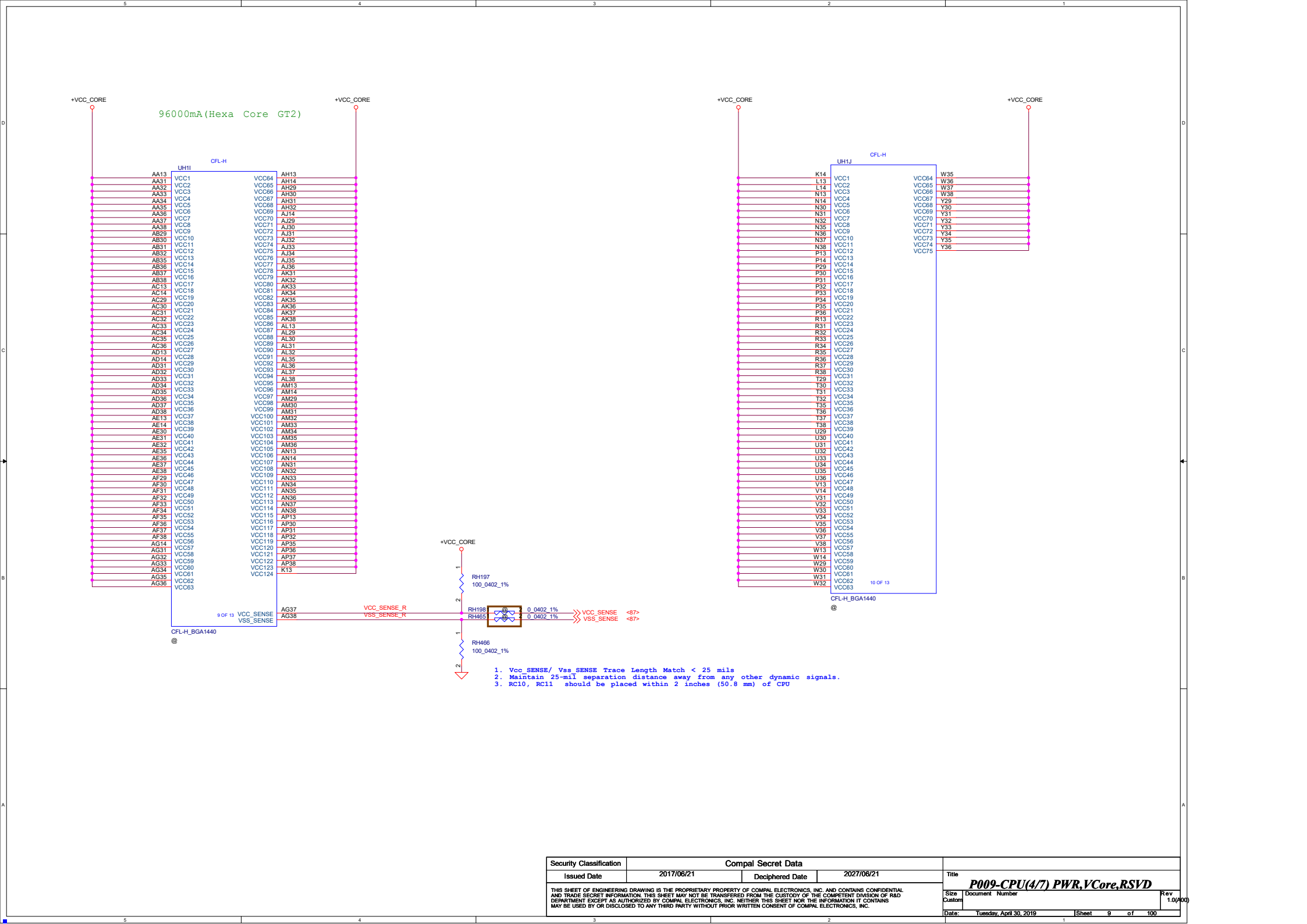


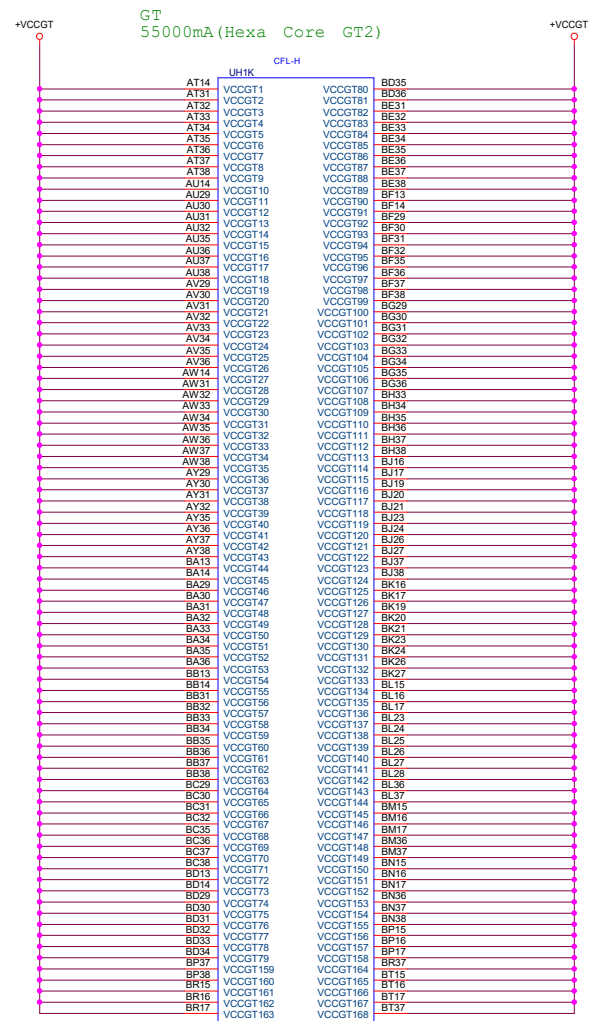
Table 2-18. PCI Required Efficiencies and User Potential Mapping																	
PCI Category	Low to High			High to High			Low to High										
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 1	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 2	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 4	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 5	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 6	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 7	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 8	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 9	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 10	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 11	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 12	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 13	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 14	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 15	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 16	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 17	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 18	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 19	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 20	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 21	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 22	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 23	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 24	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 25	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 26	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 27	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 28	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 29	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 30	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
PCI 31	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		

Notes:

1. PCI 1 is a category 1 PCI, which is a PCI that is





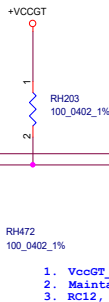


11 of VSSGT_SENSE
VCCGT_SENSE

CFL-H_BGA1440
@

AH37 VSSGT_SENSE_R RH204
AH38 VCCGT_SENSE_R RH471

0.0402 1%
0.0402 1%



Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/06/21	Deciphered Date	2021/06/21	Title
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Size	Document	Number	Rev	1.0/100
Custom				
Date:	Tuesday, April 30, 2019	Sheet	11 of 100	

CFL-H		
UH1F		
A10	VSS_1	VSS_82
A12	VSS_2	VSS_83
A16	VSS_3	VSS_84
A18	VSS_4	VSS_85
A20	VSS_5	VSS_86
A22	VSS_6	VSS_87
A24	VSS_7	VSS_88
A26	VSS_8	VSS_89
A28	VSS_9	VSS_90
A30	VSS_10	VSS_91
A6	VSS_11	VSS_92
A9	VSS_12	VSS_93
AA12	VSS_13	VSS_94
AA29	VSS_14	VSS_95
AA30	VSS_15	VSS_96
AB33	VSS_16	VSS_97
AB34	VSS_17	VSS_98
AB5	VSS_18	VSS_99
AC1	VSS_19	VSS_100
AC12	VSS_20	VSS_101
AC2	VSS_21	VSS_102
AC3	VSS_22	VSS_103
AC37	VSS_23	VSS_104
AC38	VSS_24	VSS_105
AC4	VSS_25	VSS_106
AC5	VSS_26	VSS_107
AC6	VSS_27	VSS_108
AD10	VSS_28	VSS_109
AD11	VSS_29	VSS_110
AD12	VSS_30	VSS_111
AD29	VSS_31	VSS_112
AD30	VSS_32	VSS_113
AD6	VSS_33	VSS_114
AD8	VSS_34	VSS_115
AD9	VSS_35	VSS_116
AE33	VSS_36	VSS_117
AE34	VSS_37	VSS_118
AE6	VSS_38	VSS_119
AF1	VSS_39	VSS_120
AF12	VSS_40	VSS_121
AF13	VSS_41	VSS_122
AF14	VSS_42	VSS_123
AF2	VSS_43	VSS_124
AF3	VSS_44	VSS_125
AF4	VSS_45	VSS_126
AG10	VSS_46	VSS_127
AG11	VSS_47	VSS_128
AG13	VSS_48	VSS_129
AG29	VSS_49	VSS_130
AG30	VSS_50	VSS_131
AG6	VSS_51	VSS_132
AG7	VSS_52	VSS_133
AG8	VSS_53	VSS_134
AH12	VSS_54	VSS_135
AH33	VSS_55	VSS_136
AH34	VSS_56	VSS_137
AH35	VSS_57	VSS_138
AH36	VSS_58	VSS_139
AH6	VSS_59	VSS_140
AJ1	VSS_60	VSS_141
AJ13	VSS_61	VSS_142
AJ2	VSS_62	VSS_143
AJ3	VSS_63	VSS_144
AJ37	VSS_64	VSS_145
AJ38	VSS_65	VSS_146
AJ4	VSS_66	VSS_147
AJ5	VSS_67	VSS_148
AJ6	VSS_68	VSS_149
W4	VSS_69	VSS_150
W5	VSS_70	VSS_151
Y10	VSS_71	VSS_152
Y11	VSS_72	VSS_153
Y13	VSS_73	VSS_154
Y14	VSS_74	VSS_155
Y37	VSS_75	VSS_156
Y38	VSS_76	VSS_157
Y7	VSS_77	VSS_158
Y8	VSS_78	VSS_159
Y9	VSS_79	VSS_160
AK29	VSS_80	VSS_161
AK30	VSS_81	VSS_162

CFL-H_BGA1440
@

CFL-H		
UH1G		
AW5	VSS_163	VSS_244
AY12	VSS_164	VSS_245
AY33	VSS_165	VSS_246
AY34	VSS_166	VSS_247
B8	VSS_167	VSS_248
BA10	VSS_168	VSS_249
BA11	VSS_169	VSS_250
BA12	VSS_170	VSS_251
BA37	VSS_171	VSS_252
BA38	VSS_172	VSS_253
BA6	VSS_173	VSS_254
BA7	VSS_174	VSS_255
BA8	VSS_175	VSS_256
BA9	VSS_176	VSS_257
BB1	VSS_177	VSS_258
BB2	VSS_178	VSS_259
BB29	VSS_179	VSS_260
BB3	VSS_180	VSS_261
BB30	VSS_181	VSS_262
BB5	VSS_182	VSS_263
BB4	VSS_183	VSS_264
BB5	VSS_184	VSS_265
BB6	VSS_185	VSS_266
BC12	VSS_186	VSS_267
BC13	VSS_187	VSS_268
BC14	VSS_188	VSS_269
BC33	VSS_189	VSS_270
BC34	VSS_190	VSS_271
BC6	VSS_191	VSS_272
BD10	VSS_192	VSS_273
BD11	VSS_193	VSS_274
BD12	VSS_194	VSS_275
BD37	VSS_195	VSS_276
BD6	VSS_196	VSS_277
BD7	VSS_197	VSS_278
BD8	VSS_198	VSS_279
BD9	VSS_199	VSS_280
BE1	VSS_200	VSS_281
BE2	VSS_201	VSS_282
BE29	VSS_202	VSS_283
BE3	VSS_203	VSS_284
BE30	VSS_204	VSS_285
BE4	VSS_205	VSS_286
BE5	VSS_206	VSS_287
BE6	VSS_207	VSS_288
BF12	VSS_208	VSS_289
BF33	VSS_209	VSS_290
BF34	VSS_210	VSS_291
BF6	VSS_211	VSS_292
BG12	VSS_212	VSS_293
BG13	VSS_213	VSS_294
BG14	VSS_214	VSS_295
BG37	VSS_215	VSS_296
BG38	VSS_216	VSS_297
BG6	VSS_217	VSS_298
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BH8	VSS_229	VSS_310
BH9	VSS_230	VSS_311
I2	VSS_231	VSS_312
I3	VSS_232	VSS_313
T33	VSS_233	VSS_314
T34	VSS_234	VSS_315
T4	VSS_235	VSS_316
T5	VSS_236	VSS_317
T7	VSS_237	VSS_318
T8	VSS_238	VSS_319
T9	VSS_239	VSS_320
U37	VSS_240	VSS_321
U38	VSS_241	VSS_322
U39	VSS_242	VSS_323
U40	VSS_243	VSS_324

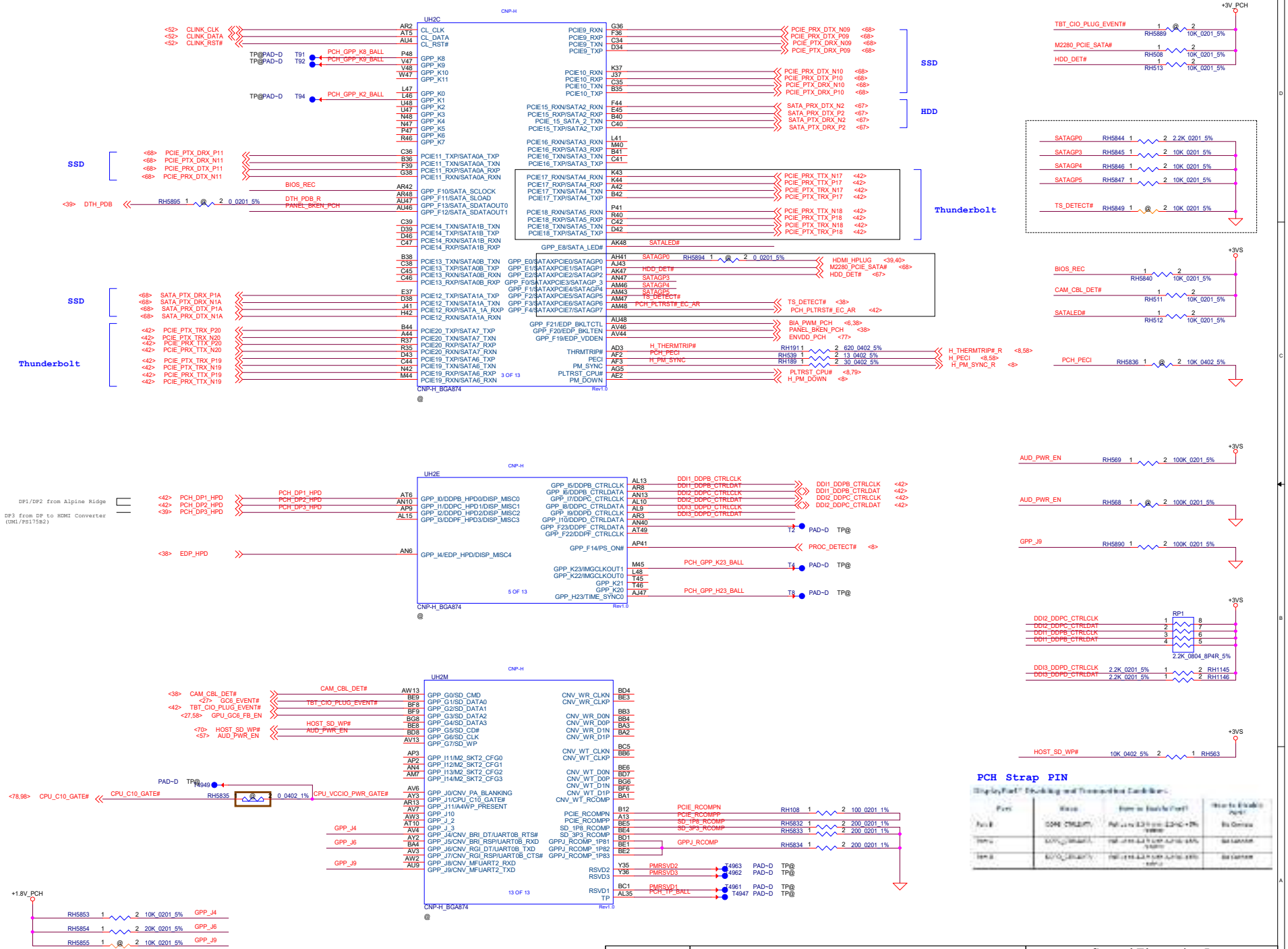
CFL-H_BGA1440
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CFL-H		
UH1H		
BN4	VSS_325	VSS_409
BN7	VSS_326	VSS_410
BP12	VSS_327	VSS_411
BP14	VSS_328	VSS_412
BP16	VSS_329	VSS_413
BP21	VSS_330	VSS_414
BP24	VSS_331	VSS_415
BP25	VSS_332	VSS_416
BP26	VSS_333	VSS_417
BP29	VSS_334	VSS_418
BP33	VSS_335	VSS_419
BP34	VSS_336	VSS_420
BP7	VSS_337	VSS_421
BR12	VSS_338	VSS_422
BR14	VSS_339	VSS_423
BR18	VSS_340	VSS_424
BR21	VSS_341	VSS_425
BR24	VSS_342	VSS_426
BR25	VSS_343	VSS_427
BR26	VSS_344	VSS_428
BR29	VSS_345	VSS_429
BR34	VSS_346	VSS_430
BR36	VSS_347	VSS_431
BT12	VSS_348	VSS_432
BT14	VSS_349	VSS_433
BT18	VSS_350	VSS_434
BT21	VSS_351	VSS_435
BT24	VSS_352	VSS_436
BT26	VSS_353	VSS_437
BT29	VSS_354	VSS_438
BT32	VSS_355	VSS_439
BT5	VSS_356	VSS_440
C11	VSS_357	VSS_441
C13	VSS_358	VSS_442
C15	VSS_359	VSS_443
C17	VSS_360	VSS_444
C19	VSS_361	VSS_445
C21	VSS_362	VSS_446
C23	VSS_363	VSS_447
C25	VSS_364	VSS_448
C26	VSS_365	VSS_449
C27	VSS_366	VSS_450
C29	VSS_367	VSS_451
C31	VSS_368	VSS_452
C37	VSS_369	VSS_453
C5	VSS_370	VSS_454
C8	VSS_371	VSS_455
C9	VSS_372	VSS_456
D10	VSS_373	VSS_457
D12	VSS_374	VSS_458
D14	VSS_375	VSS_459
D16	VSS_376	VSS_460
D18	VSS_377	VSS_461
D20	VSS_378	VSS_462
D22	VSS_379	VSS_463
D24	VSS_380	VSS_464
D26	VSS_381	VSS_465
D28	VSS_382	VSS_466
D3	VSS_383	VSS_467
D30	VSS_384	VSS_468
D33	VSS_385	VSS_469
D6	VSS_386	VSS_470
D9	VSS_387	VSS_471
E34	VSS_388	VSS_472
E35	VSS_389	VSS_473
E38	VSS_390	VSS_474
E4	VSS_391	VSS_475
E9	VSS_392	VSS_476
N3	VSS_393	VSS_477
N33	VSS_394	VSS_478
N34	VSS_395	VSS_479
N4	VSS_396	
N5	VSS_397	VSS_A3
N6	VSS_398	VSS_A4
N7	VSS_399	VSS_B3
N8	VSS_400	VSS_B3
N9	VSS_401	VSS_B37
P12	VSS_402	VSS_BR38
P37	VSS_403	VSS_BT3
M14	VSS_404	VSS_BT35
M6	VSS_405	VSS_BT36
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F11	VSS_407	VSS_C2
F13	VSS_408	VSS_D38

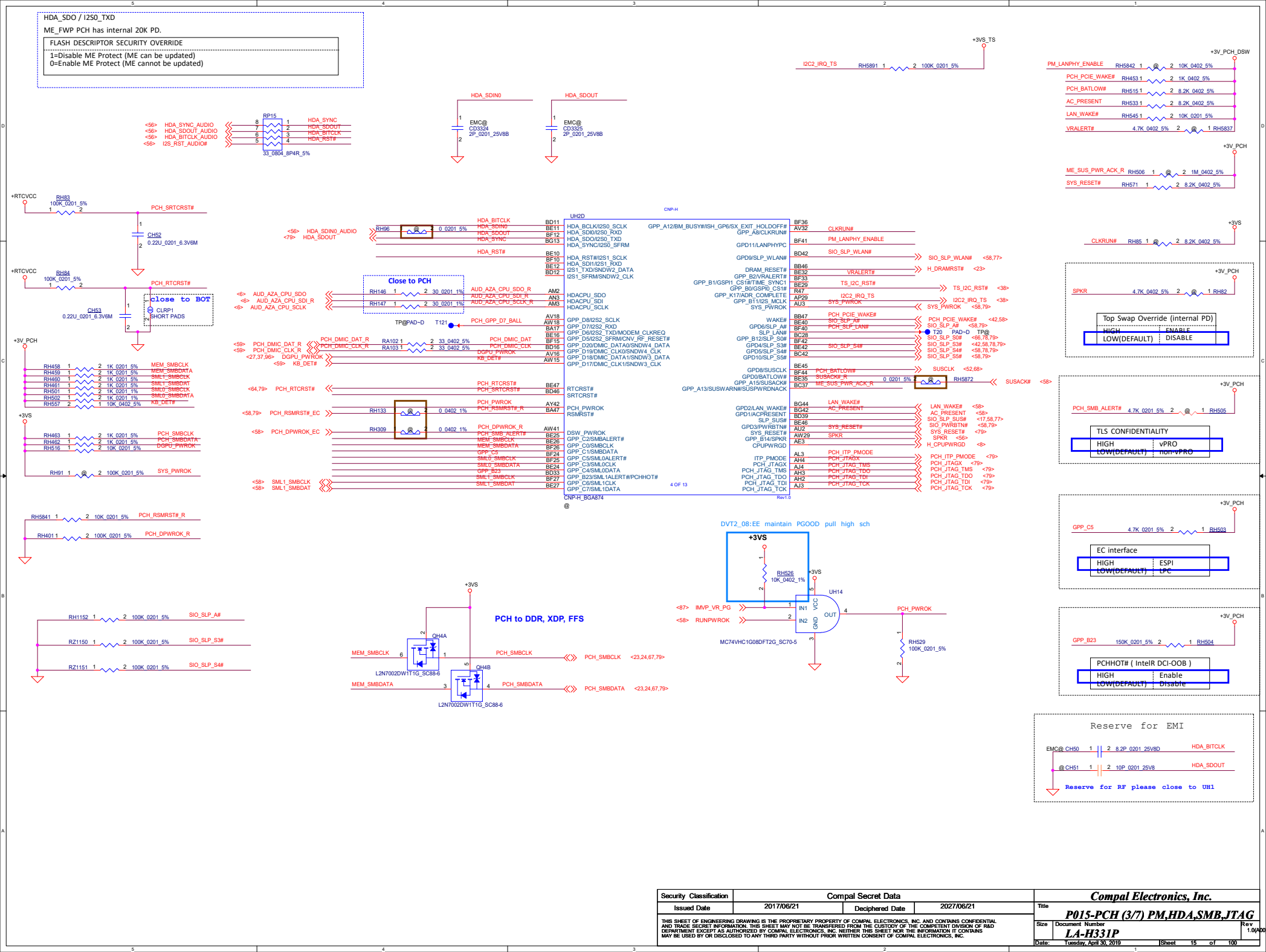
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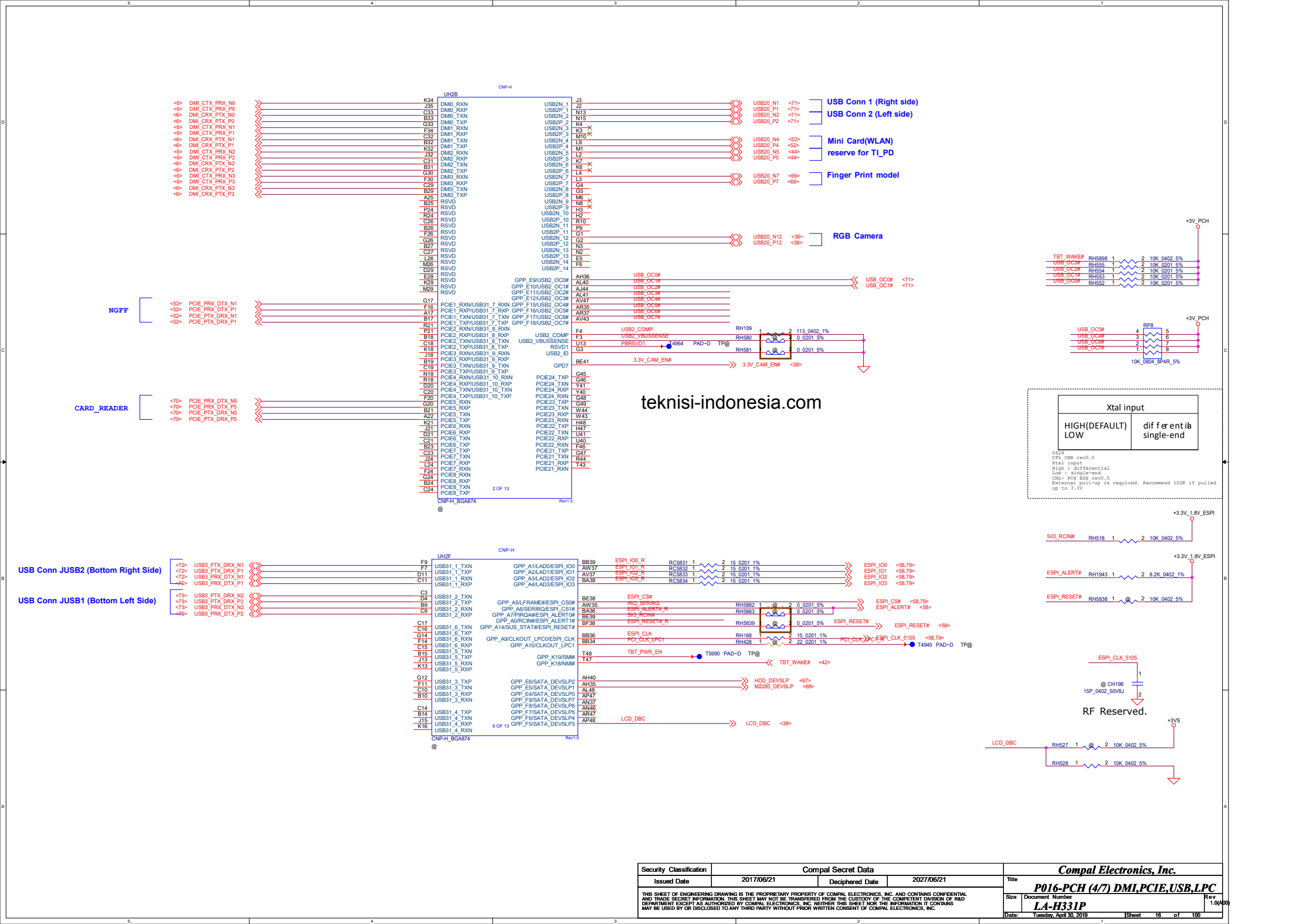
Security Classification	Compal Secret Data		Title	
Issued Date	2017/06/21	Deciphered Date	2027/06/21	2012-CPU(7/7) VSS
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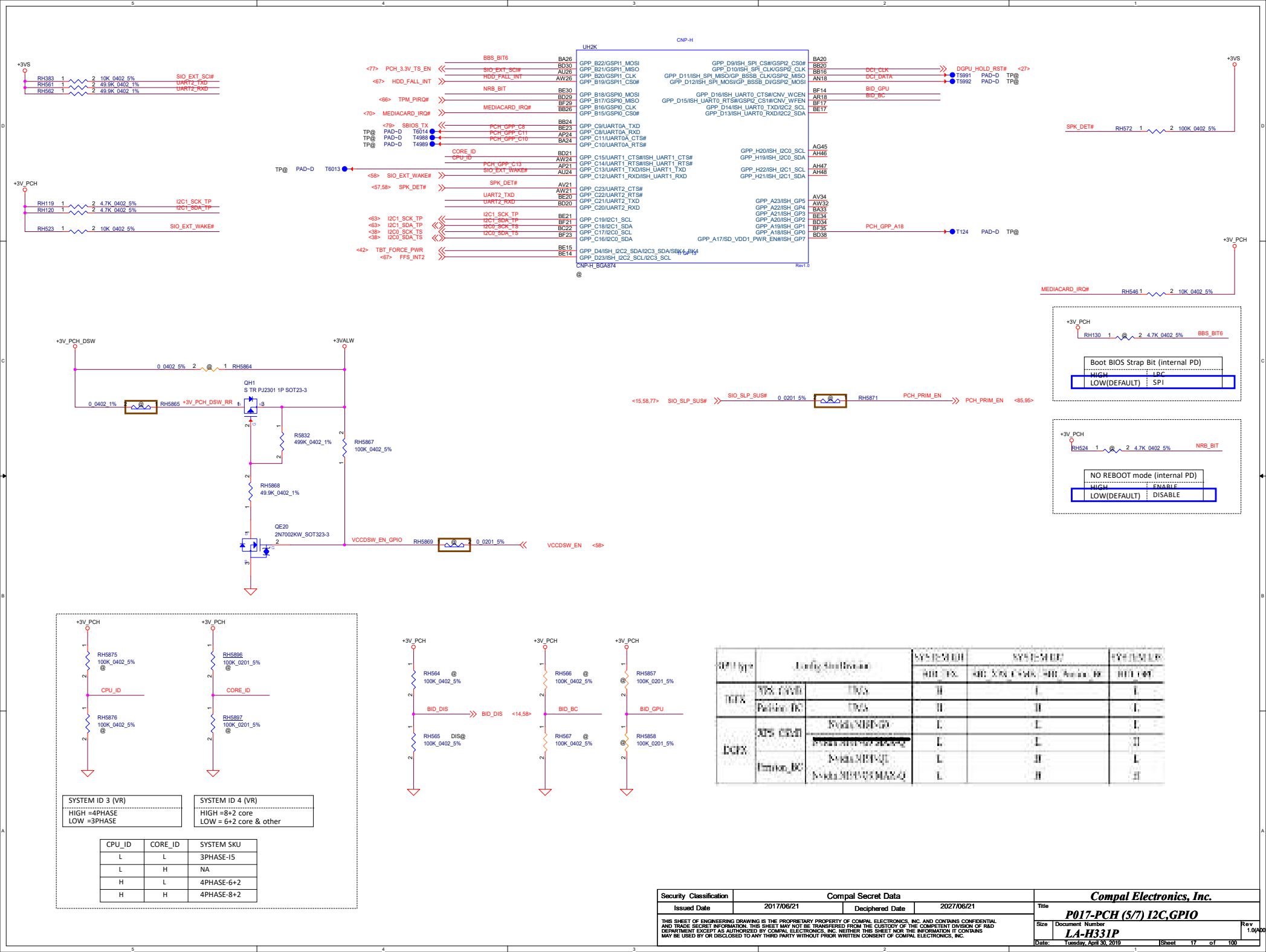


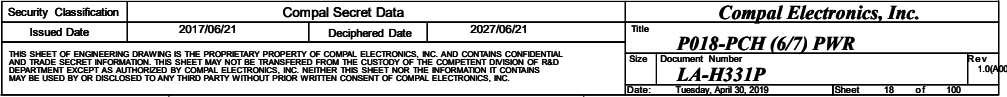


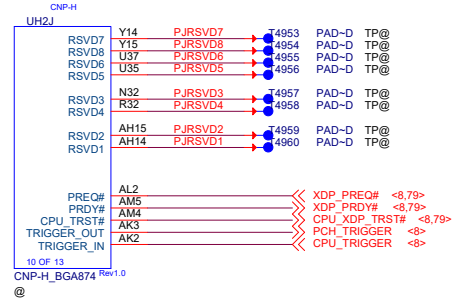
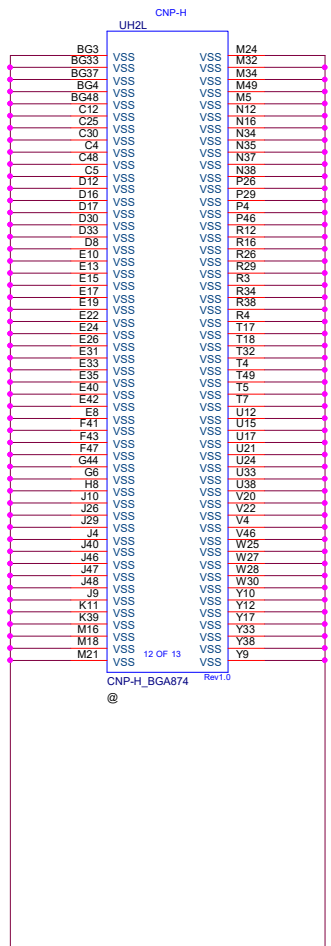
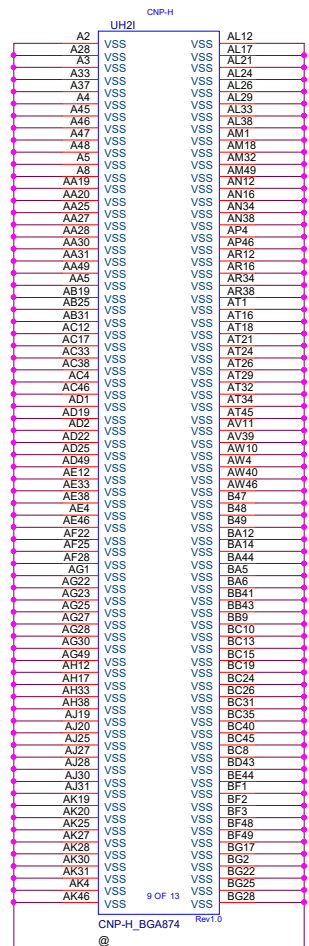


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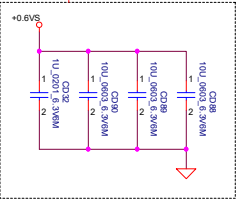
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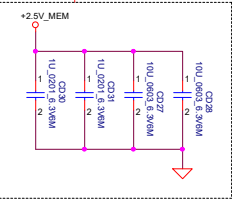
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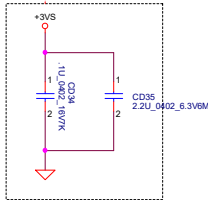
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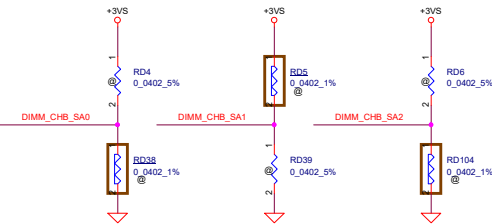
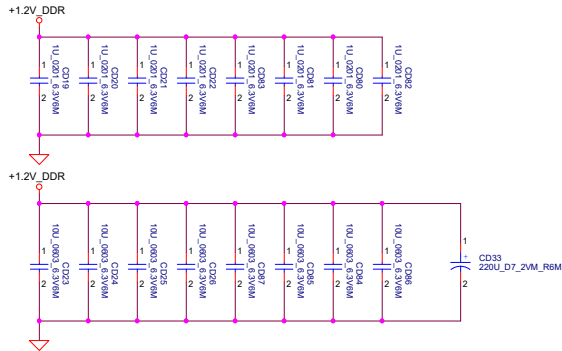
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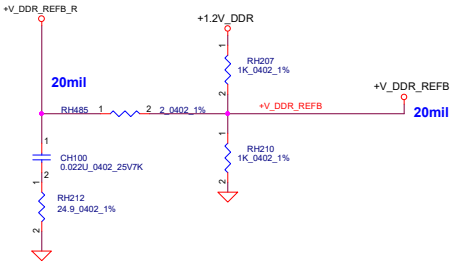
Layout Note:
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Layout Note:
Place near JDIMM5



VREF traces should be at least 20 mils wide with 20 mils spacing to other signals



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<7> DDR_B_MA0[13]
<7> DDR_B_DQS#0[7]
<7> DDR_B_DQS#0[7]

<7> DDR_CKE2_DIMMB#

<7> DDR_B_BG1

<7> DDR_B_BG0

<7> M_CLK_DDR2

<7> M_CLK_DDR#2

<7> DDR_B_PAR

<7> DDR_B_SS1

<7> DDR_CS2_DIMMB#

<7> DDR_B_WE1

<7> M_ODT2

<7> DDR_CS3_DIMMB#

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<7> M_ODT3

<7> M_ODT3

<7> M_ODT3

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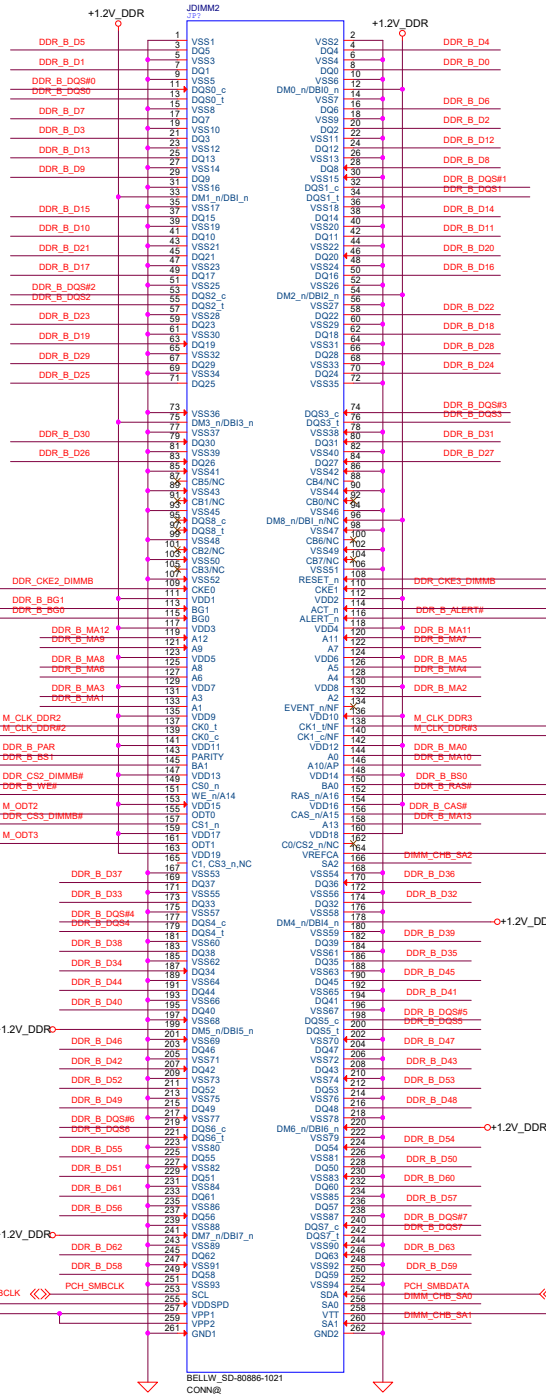
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All VREF traces should have 10 mil trace width

+V_DDR_REFB 20mil

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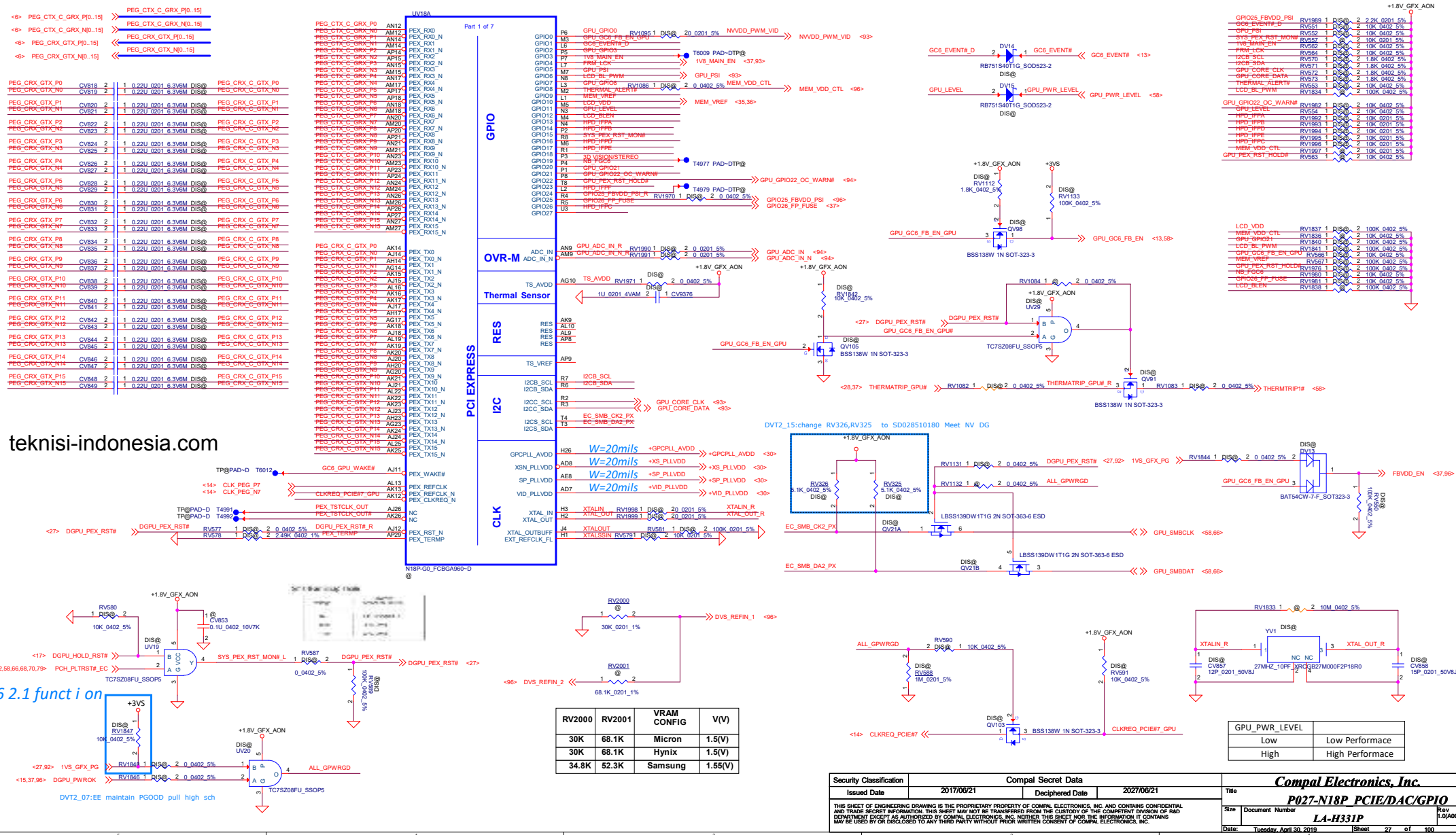
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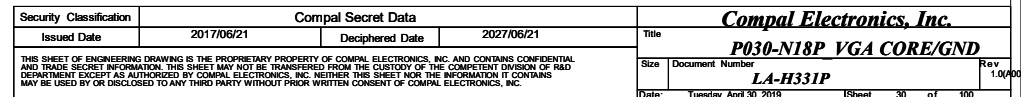
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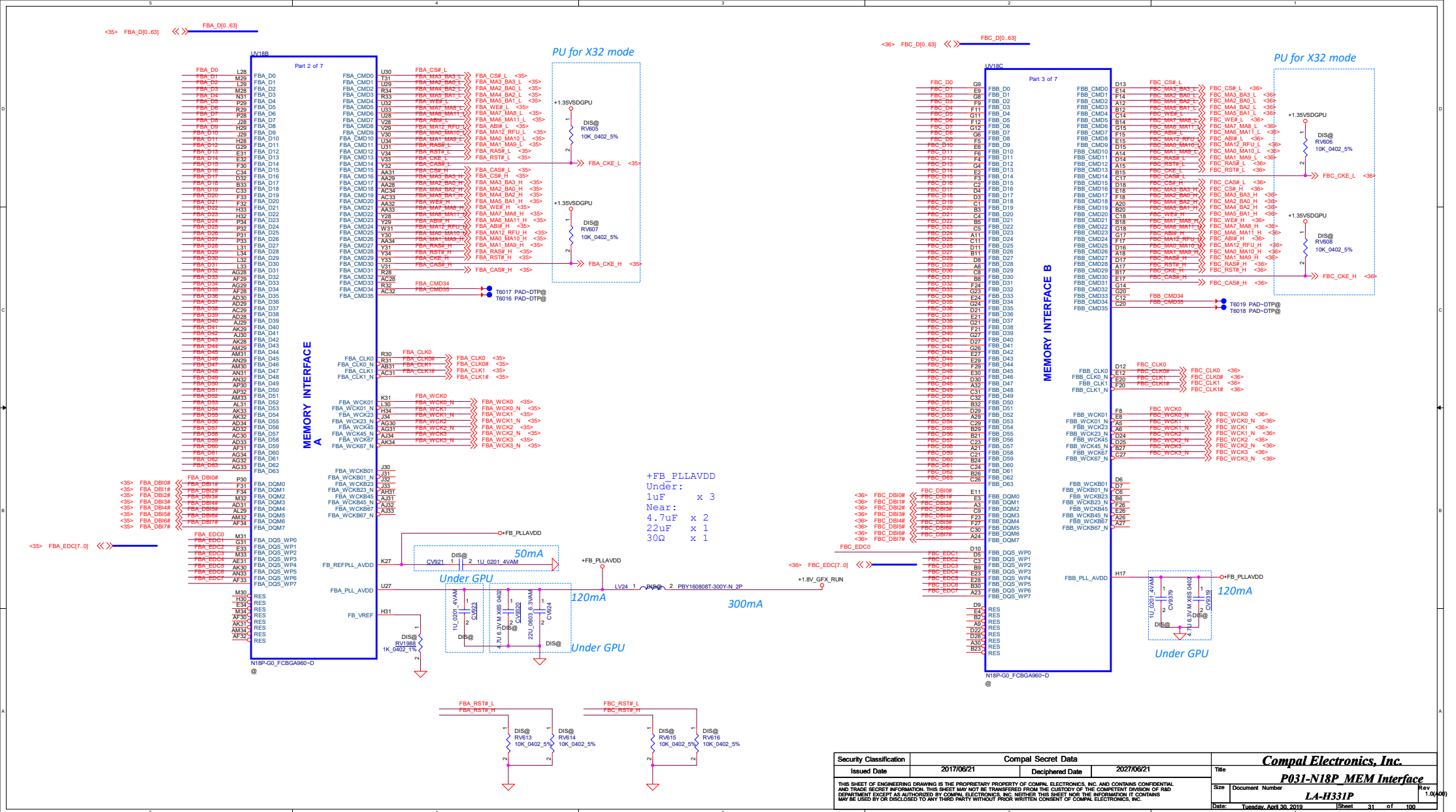
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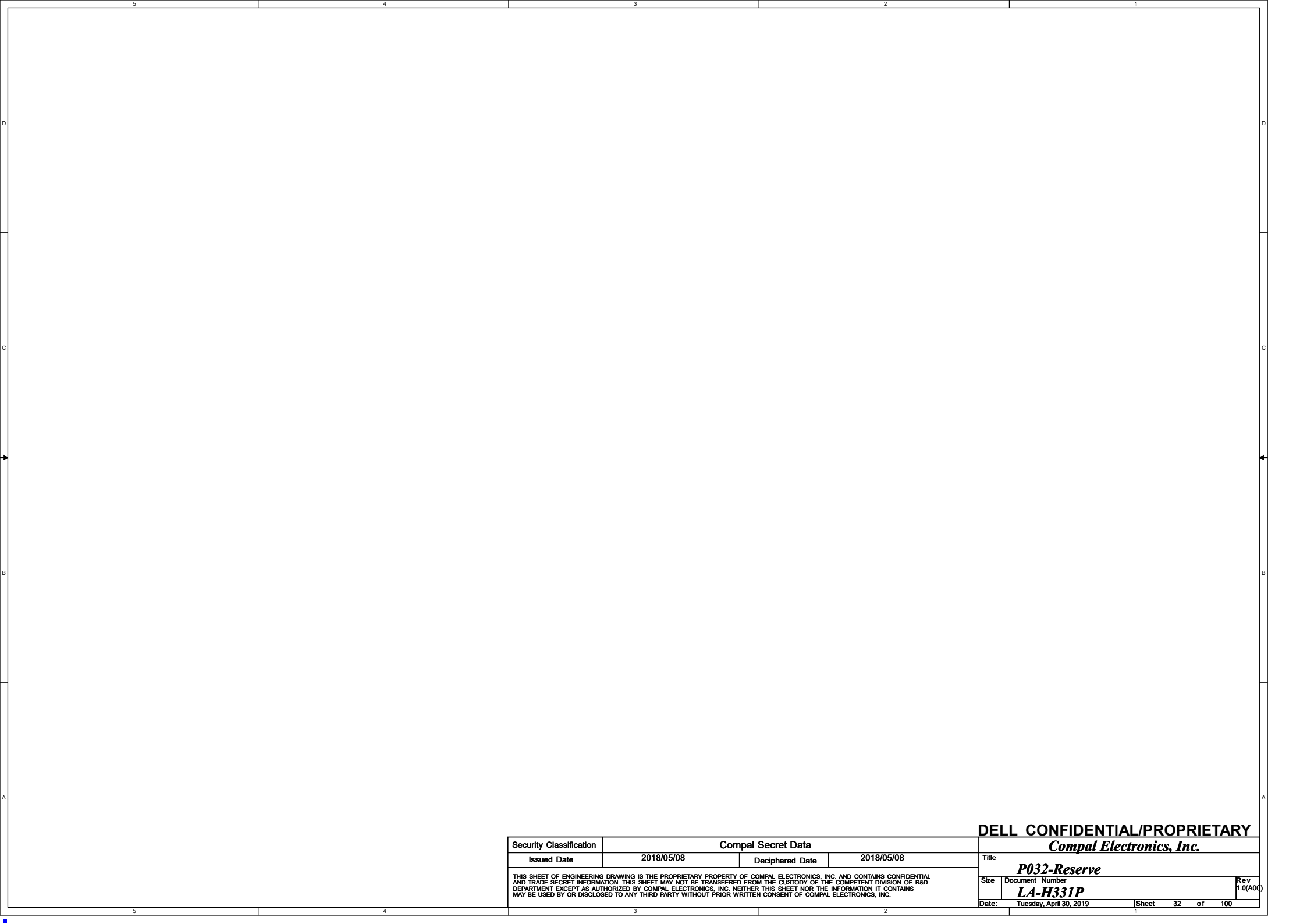
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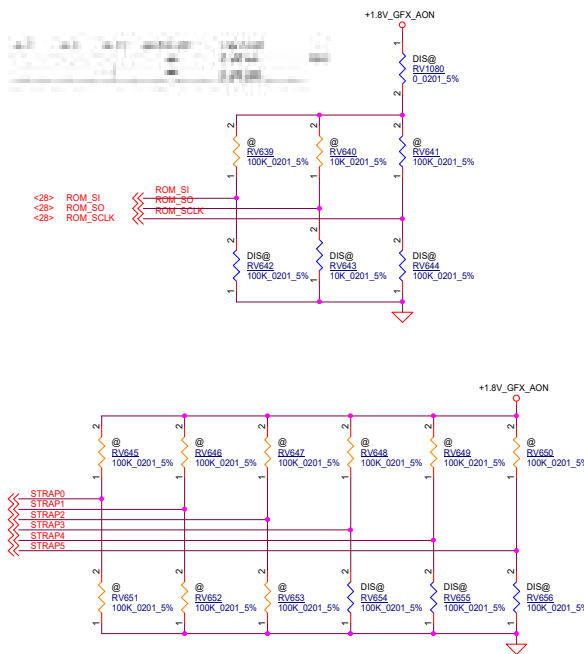


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SMB_ALT_ADDR	State	DEVID_SEL	State	PCIE_CFG	State	VGA_DEVICE	State
Low	Single GPU	Low	Original Device	Low	Normal signal swing	Low	3D Device
High	Dual GPU	High	Re-brand Device ID	High	Reduce the signal amplitude	High	VGA Device

Table 5.5 SMB_ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

Table 5.2 RAMCFG

Strap Pins see Note			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
L	L	L	0 (0x0000)	RAMCFG0
L	L	H	1 (0x0001)	RAMCFG1
L	H	L	2 (0x0002)	RAMCFG2

Table 4. N18P-Q3/G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBW/DQ	Vendor	Manufacturer Part Number	Die Revision	Speed	Memory Speed Grade	Date Code	Qual Plan	Status
8 Gb	256Mb-32	1.25V and 1.5V	Hyundai	H5G28128R4R-030	0-04	8 Gb	8 Gbps	H1A	Full	Production candidate
			Hyundai	H5G28128R4R-030	0-04	8 Gb	8 Gbps	H1A	Full	Production candidate

Notes:

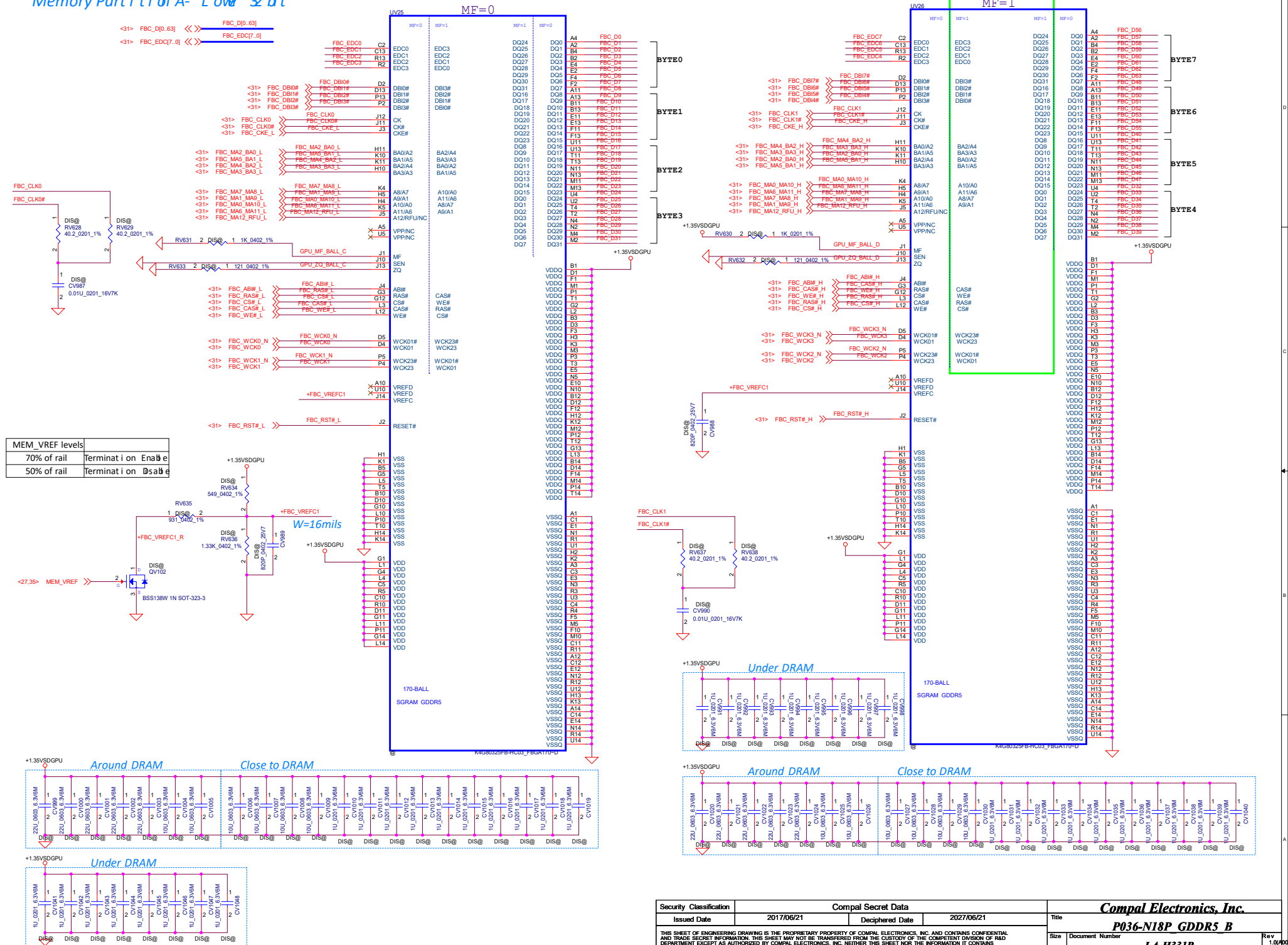
- For N18P-Q3/G1, the maximum allowable memory case temperature is 85 °C.
- FBW may be required to run WCLX > 3500 Mbit/s. TBD.

Table 5.3. GB28-64, GB48-128 and GB88-256 Multi-Wire Mode Strapping

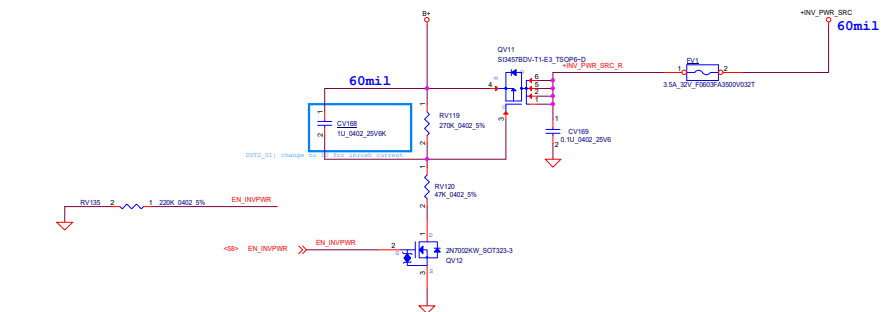
Strap Pin Name	Logical Strapping Bit 0	Logical Strapping Bit 1	Logical Strapping Bit 2	Logical Strapping Bit 3
ROM_SCL	ROM_CFG[0]	ROM_CFG[1]	ROM_CFG[2]	ROM_CFG[3]
ROM_SI	ROM_CFG[0]	ROM_CFG[1]	ROM_CFG[2]	ROM_CFG[3]
ROM_SO	ROM_CFG[0]	ROM_CFG[1]	ROM_CFG[2]	ROM_CFG[3]
STRAP0	Deep test print for pull-up to VDD_AON and pull-down to GND. Default: 45.7 kOhm up.			
STRAP1	Deep test print for pull-up to VDD_AON and pull-down to GND. Default: 45.7 kOhm up.			
STRAP2				
STRAP3				
STRAP4				

Strap Pin Name	Logical Strapping Bit 0	Logical Strapping Bit 1	Logical Strapping Bit 2	Logical Strapping Bit 3
STRAP0	STRAP_CFG[0]	STRAP_CFG[1]	STRAP_CFG[2]	STRAP_CFG[3]
STRAP1	STRAP_CFG[0]	STRAP_CFG[1]	STRAP_CFG[2]	STRAP_CFG[3]
STRAP2	STRAP_CFG[0]	STRAP_CFG[1]	STRAP_CFG[2]	STRAP_CFG[3]
STRAP3	STRAP_CFG[0]	STRAP_CFG[1]	STRAP_CFG[2]	STRAP_CFG[3]
STRAP4	STRAP_CFG[0]	STRAP_CFG[1]	STRAP_CFG[2]	STRAP_CFG[3]

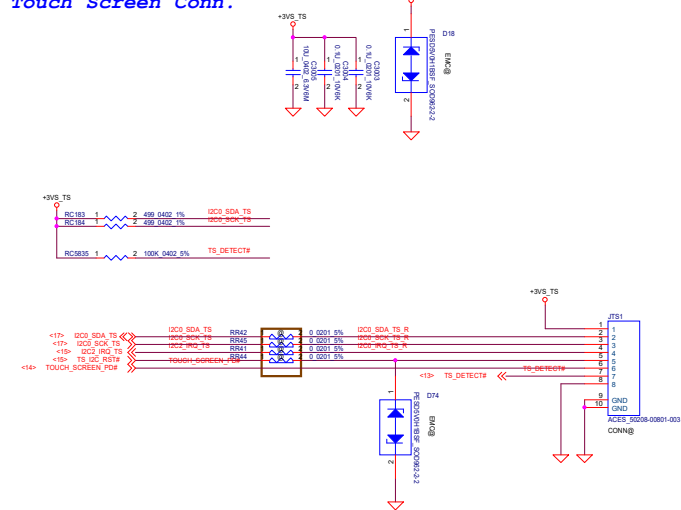
Memory Partition A- Lower 32 bit



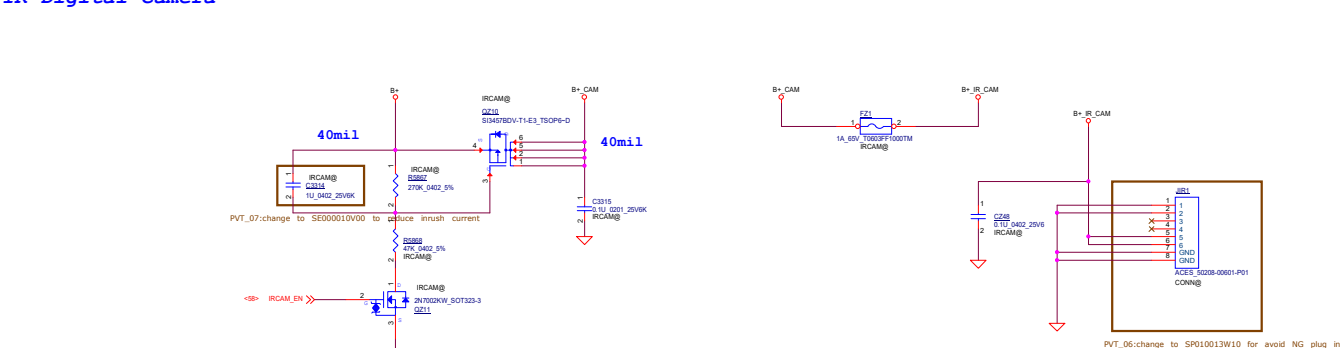
LCD backlight PWR CTRL



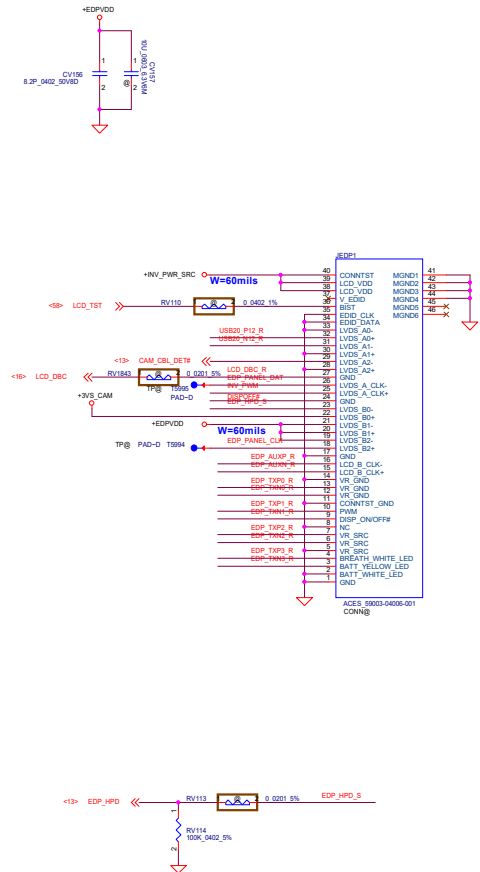
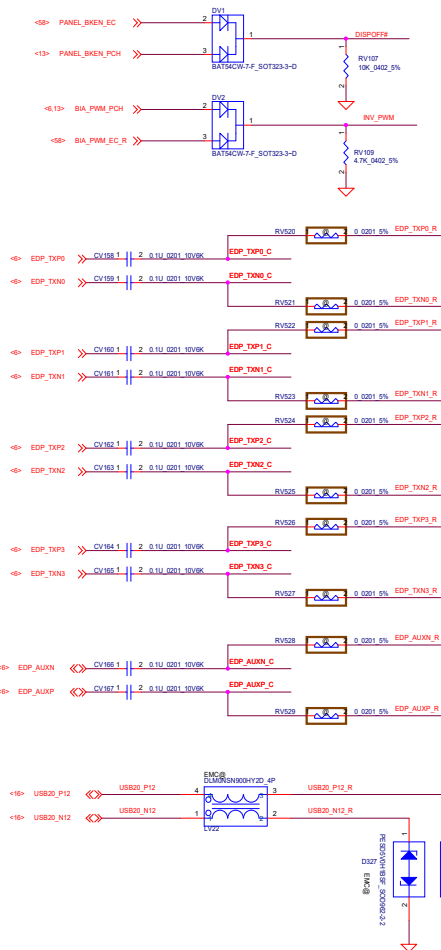
Touch Screen Conn.



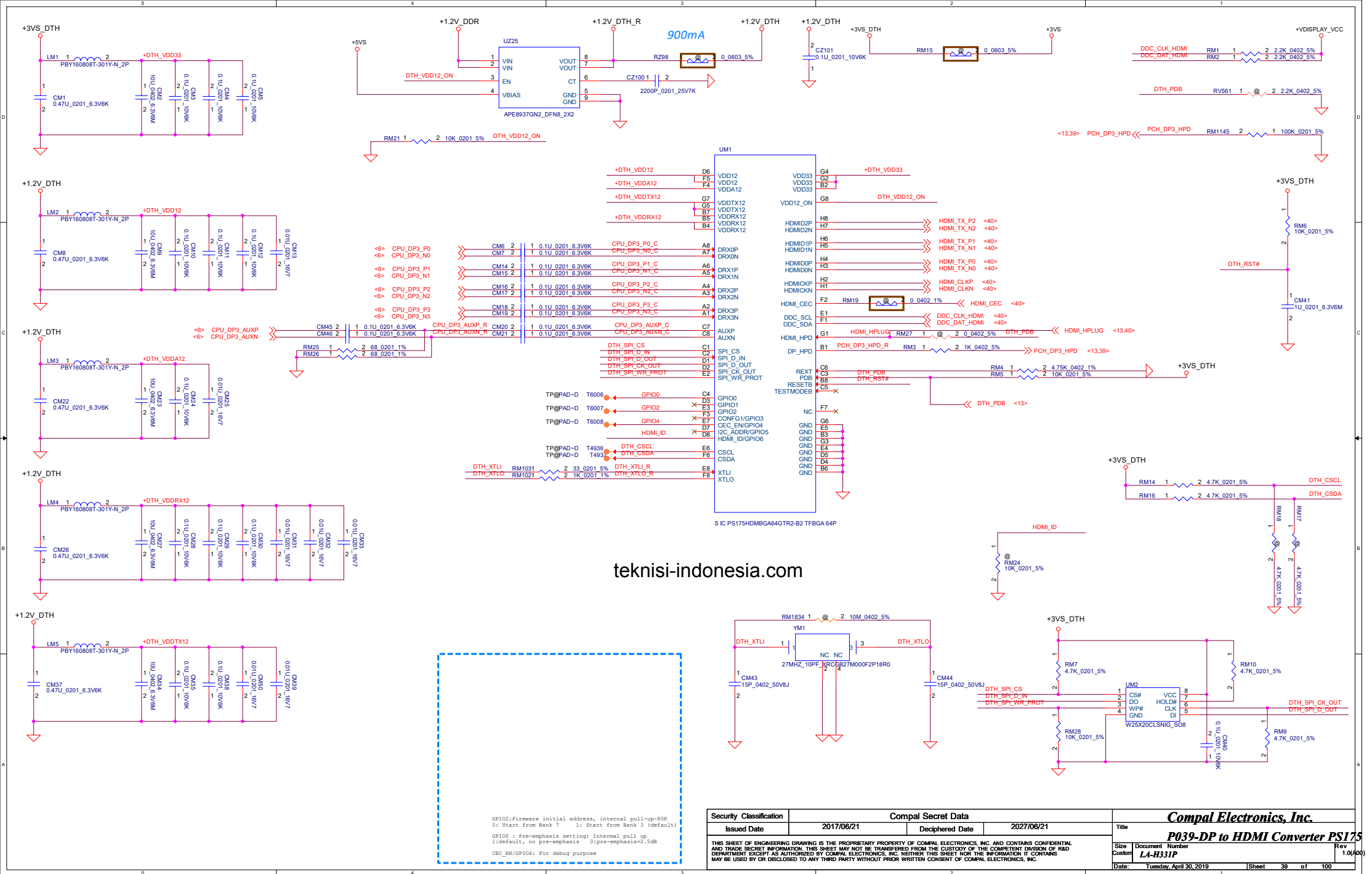
IR Digital Camera



eDP & CCD(RGB) Conn.



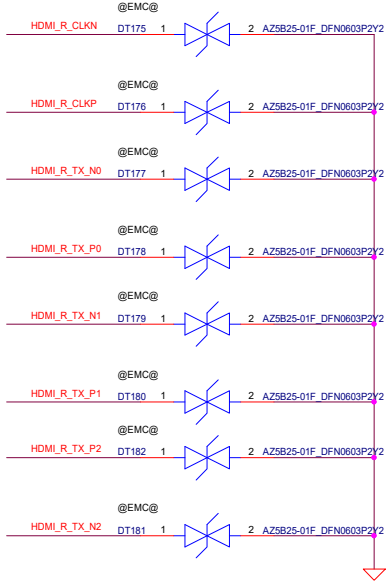
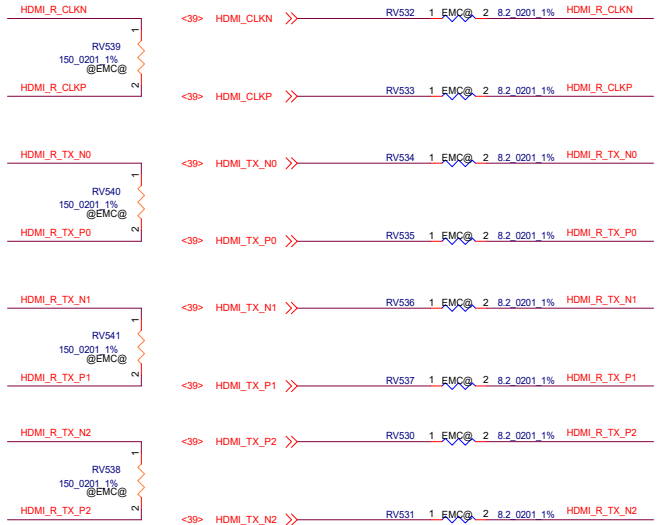
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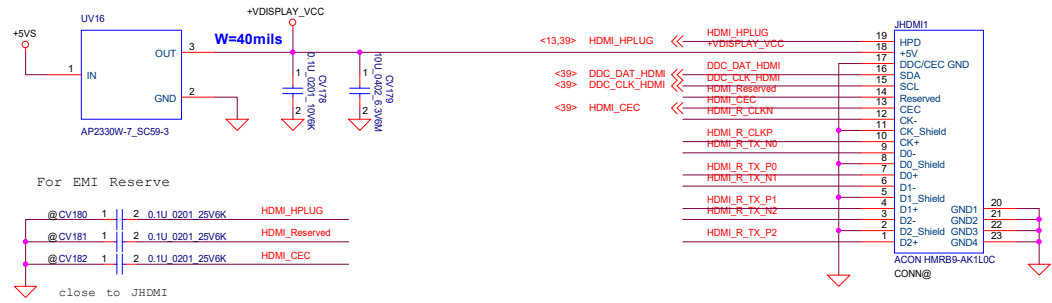
HDMI change to CPU to PS185 to CONN

Place between ESD and CM-Choke

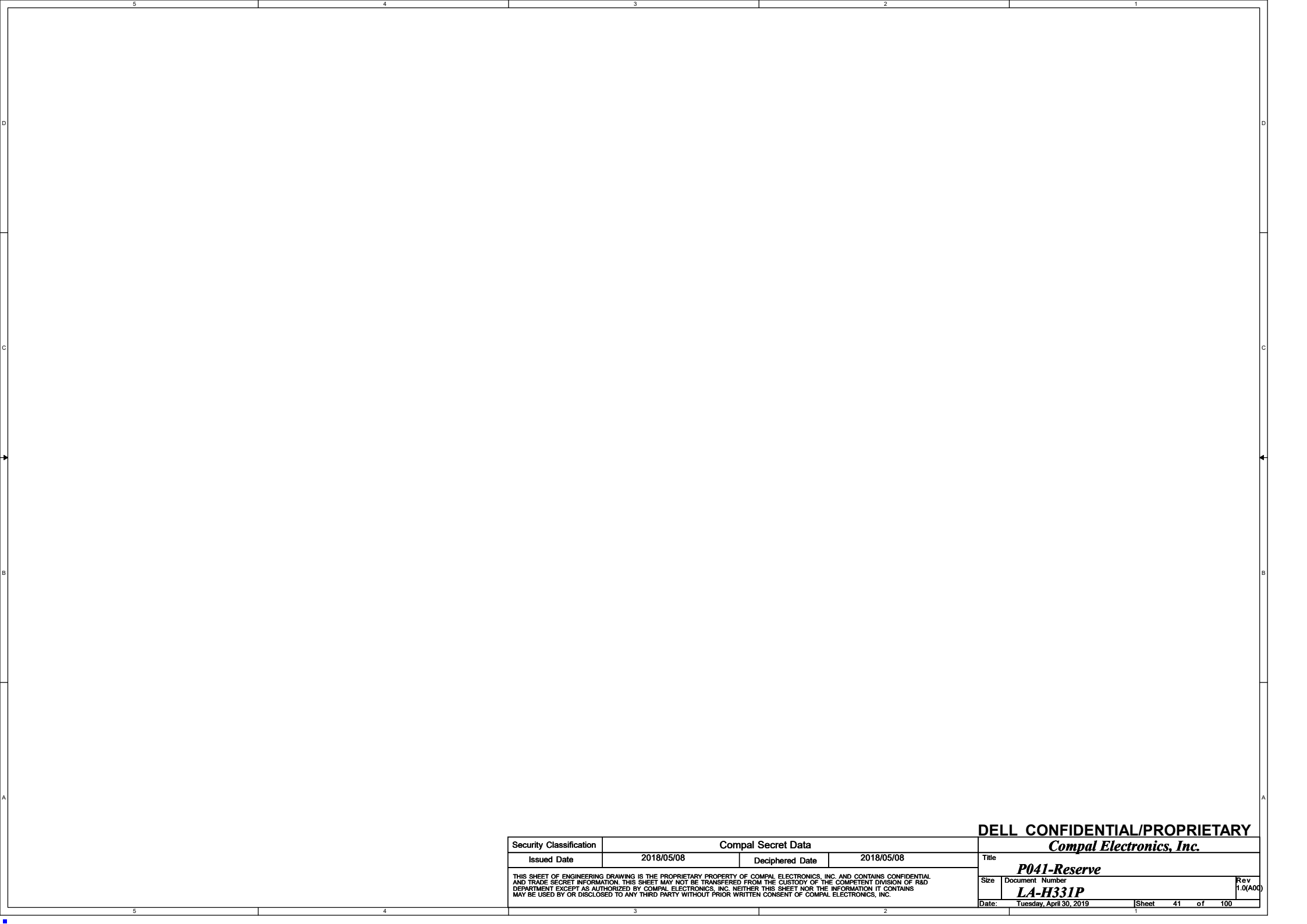
Place close to JHDMI1



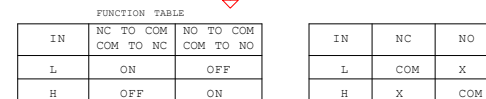
HDMI conn



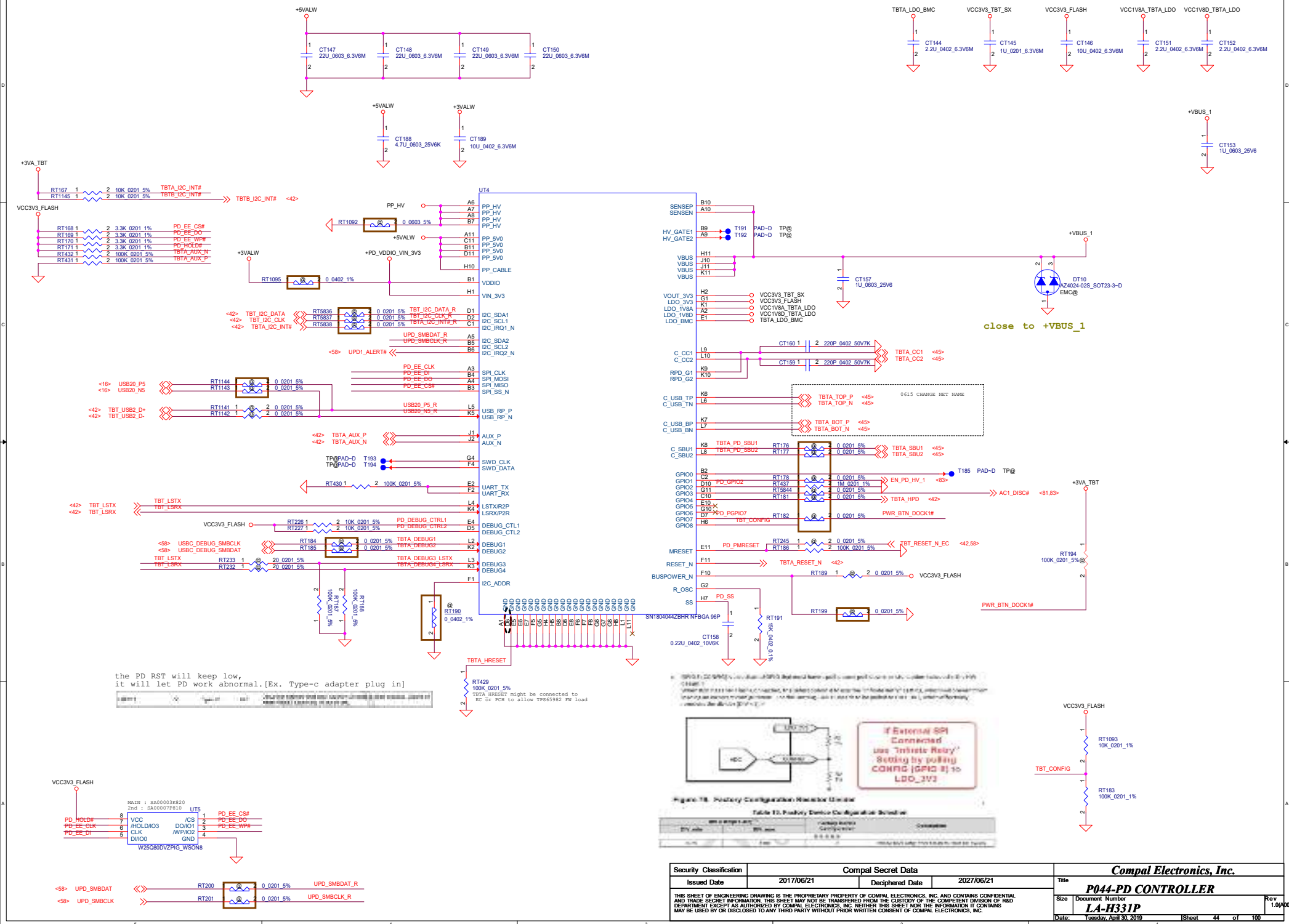
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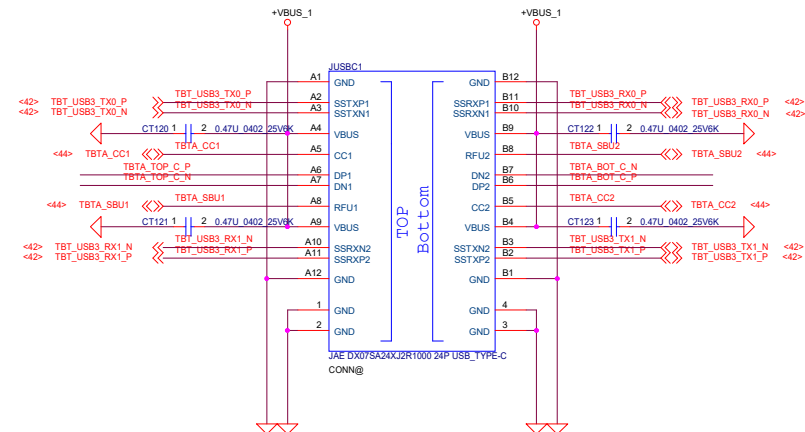
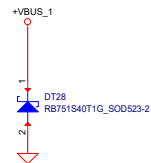
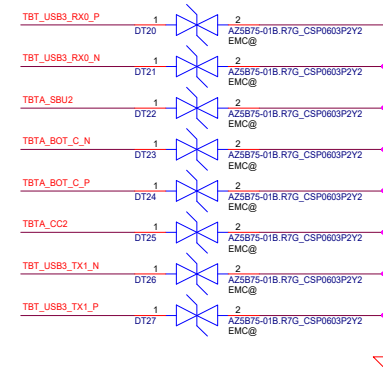
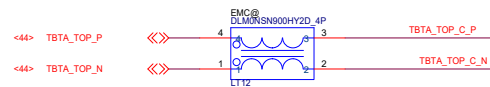


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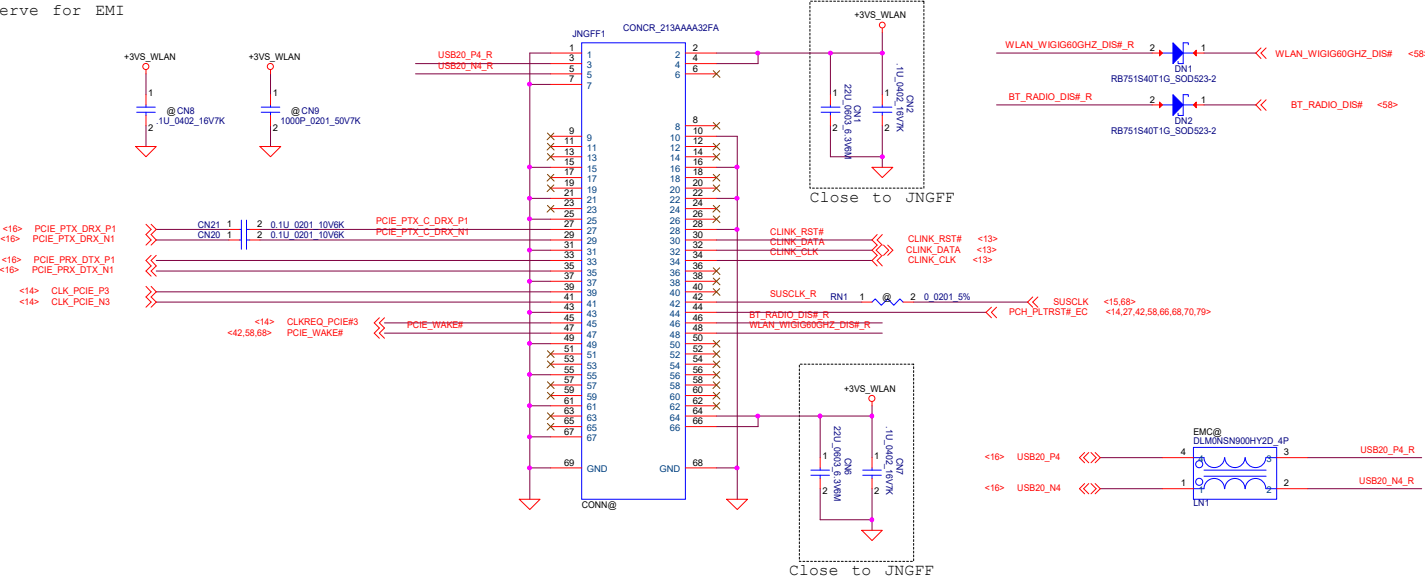
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		Issued Date	2018/05/08	Deciphered Date
		2018/05/08		
		Title		P050-Reserve
		Size	Document Number	Rev
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M.2 Slot-A Key-A (WLAN + BT)

Reserve for EMI





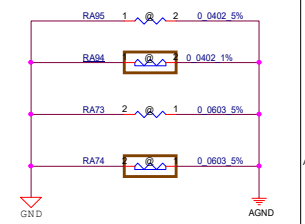
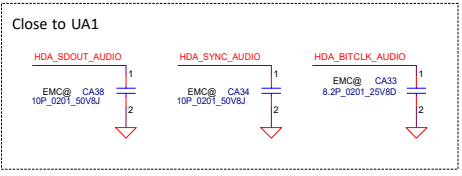
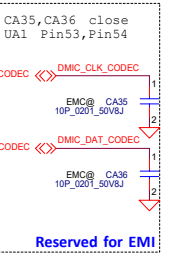
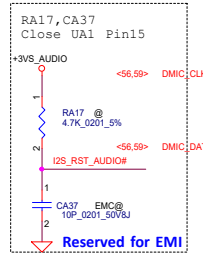
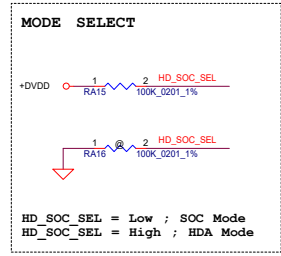
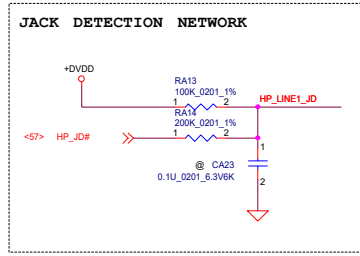
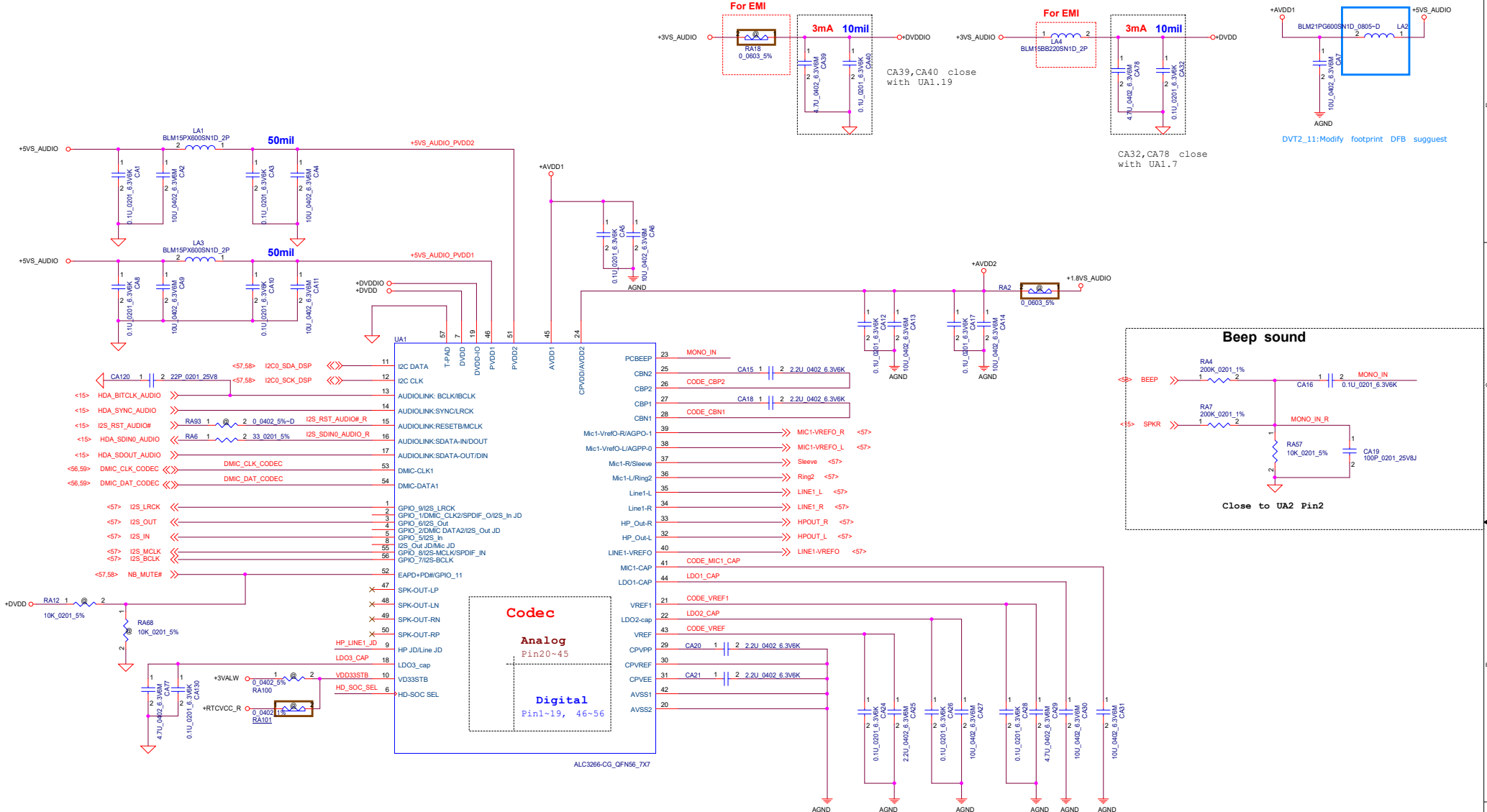
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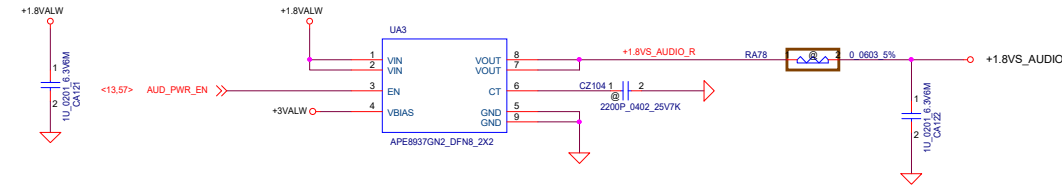


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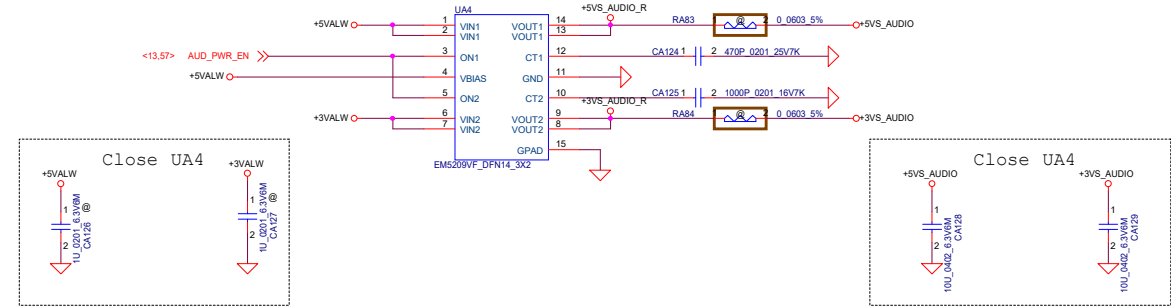


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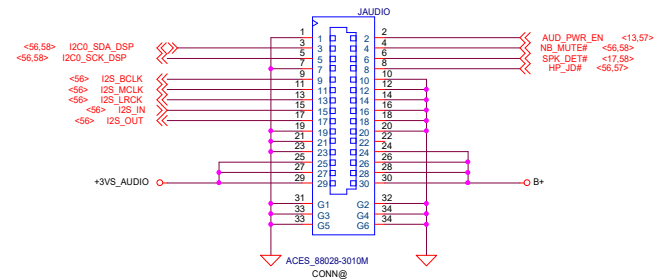
+1.8VALW To +1.8VS_AUDIO



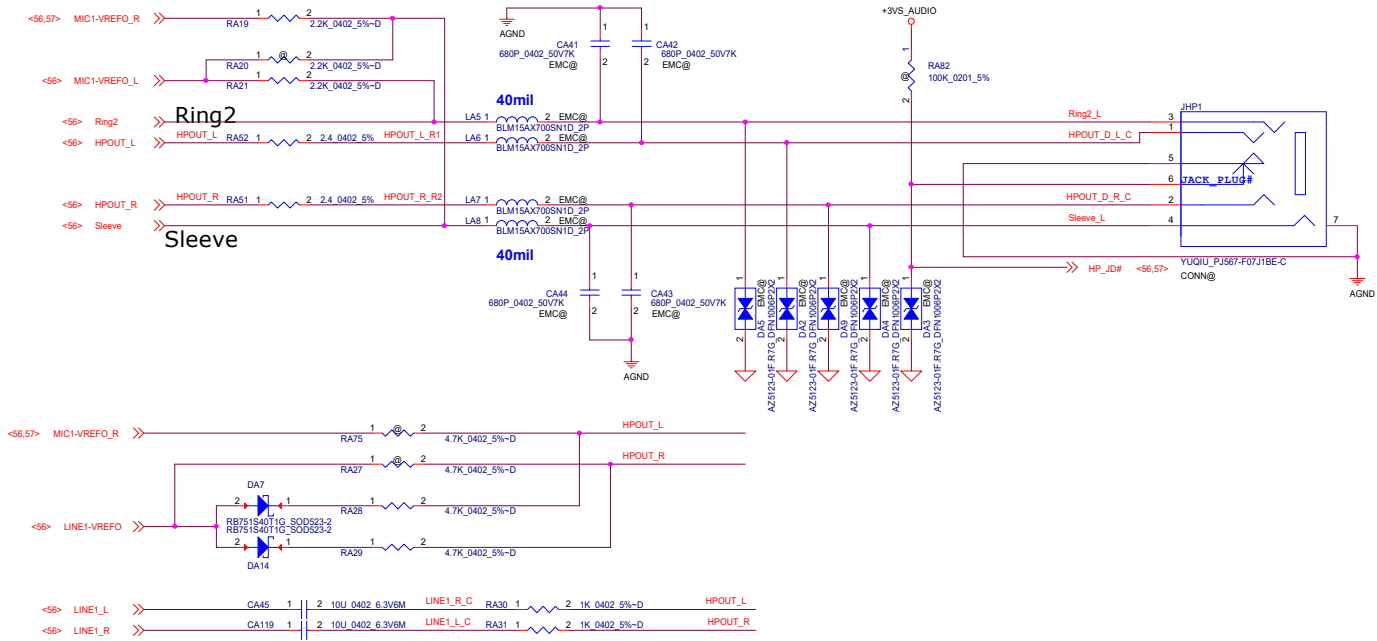
+5VALW and +3VALW To +5VS_AUDIO and +3VS_AUDIO



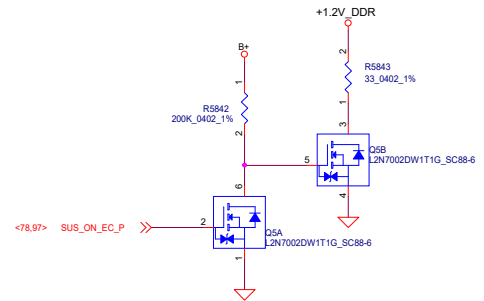
AUDIO Board Conn.



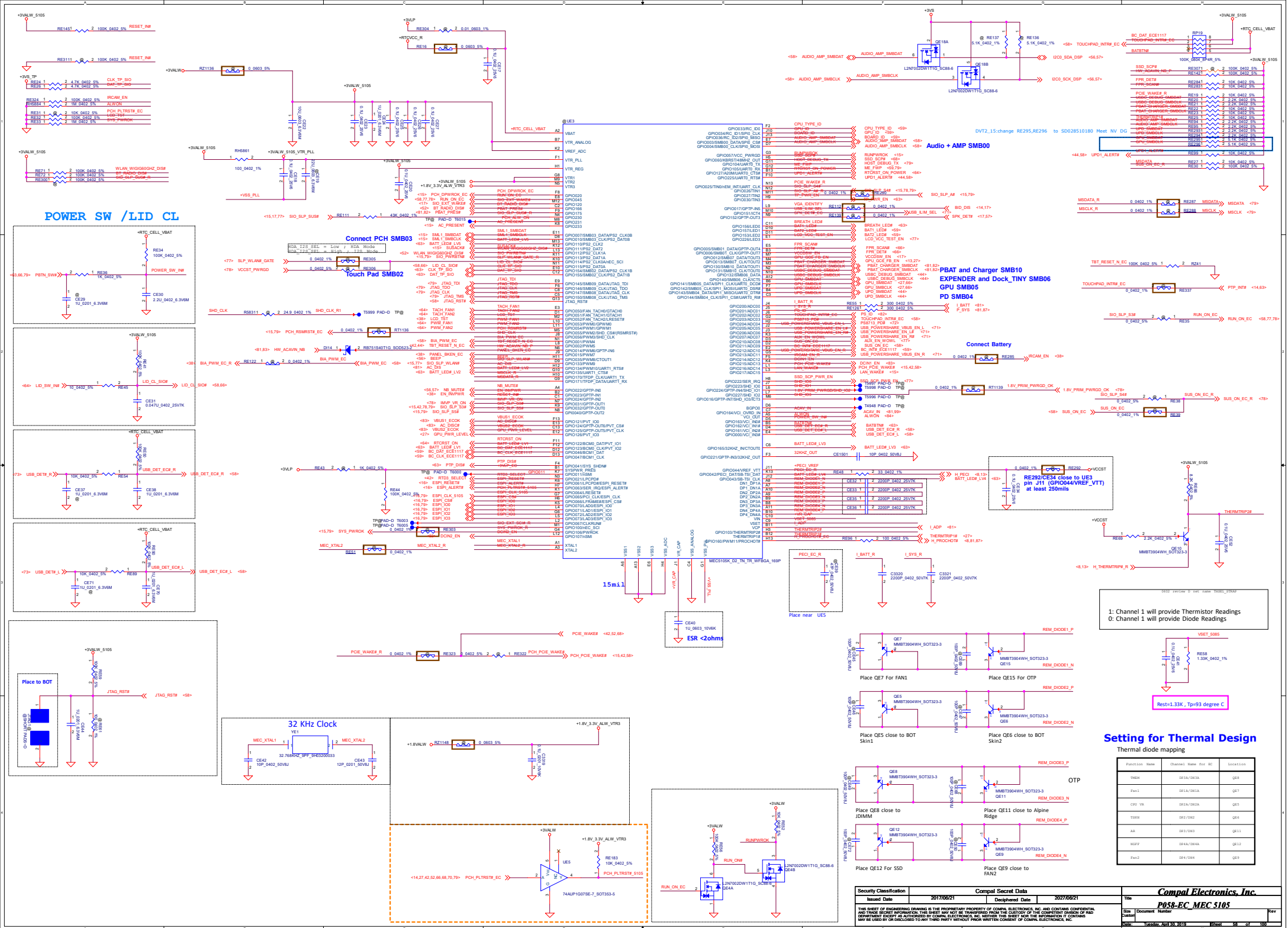
Universal Audio Jack



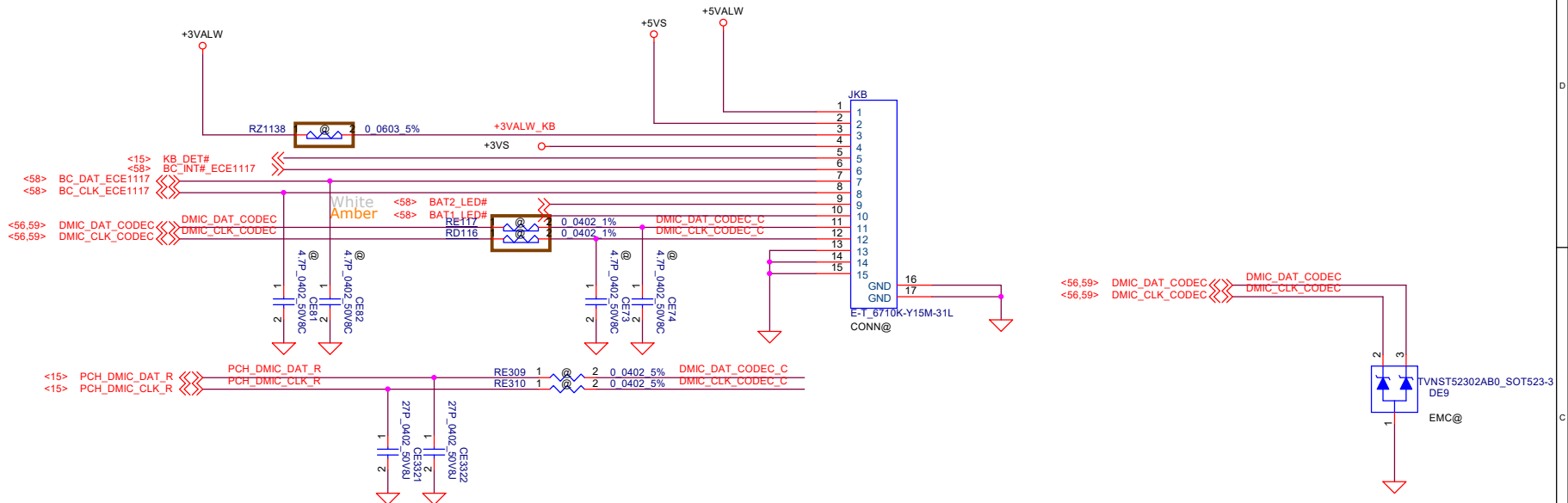
1.2V DDR discharger



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Keyboard Controller board + DMIC



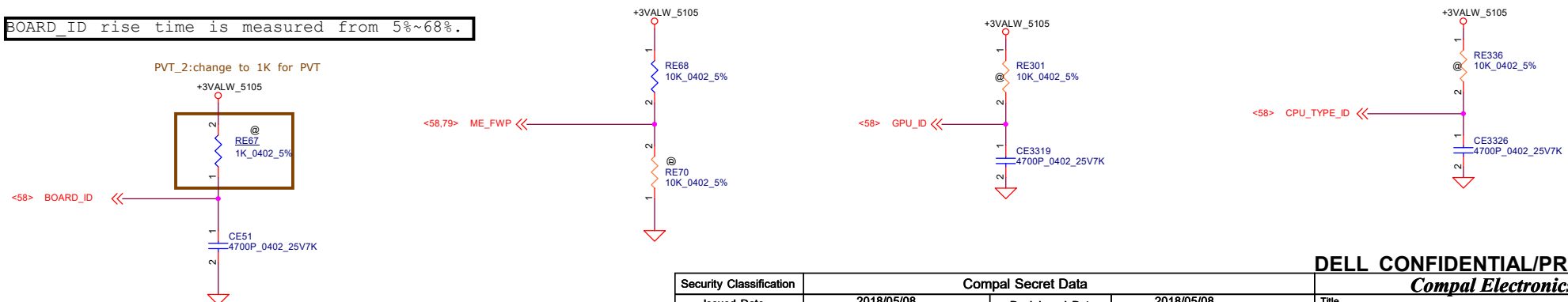
EC Strap

RE67	CE51	REV	PHASE
240K	4700p		PRE EVT
130K	4700p	X00	EVT
62K	4700p	X01	DVT1
33K	4700p	X02	DVT2
8.2K	4700p		
4.3K	4700p		
2K	4700p		
1K	4700p	A00	PVT

RE301	CE3319	CONFIG
240K	4700p	
130K	4700p	UMA
62K	4700p	N18P-G0
33K	4700p	
8.2K	4700p	N19P-Q1
4.3K	4700p	N19P-Q3 MAXQ
2K	4700p	
1K	4700p	

RE336	CE3326	CONFIG
240K	4700p	
130K	4700p	3PHASE-I5
62K	4700p	
33K	4700p	
8.2K	4700p	4PHASE-6+2
4.3K	4700p	
2K	4700p	
1K	4700p	4PHASE-8+2

BOARD_ID rise time is measured from 5%~68%.



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								P059-KBC Board			
								Size			
								Document Number			
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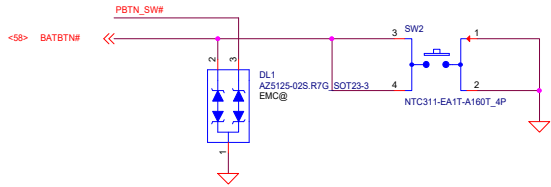
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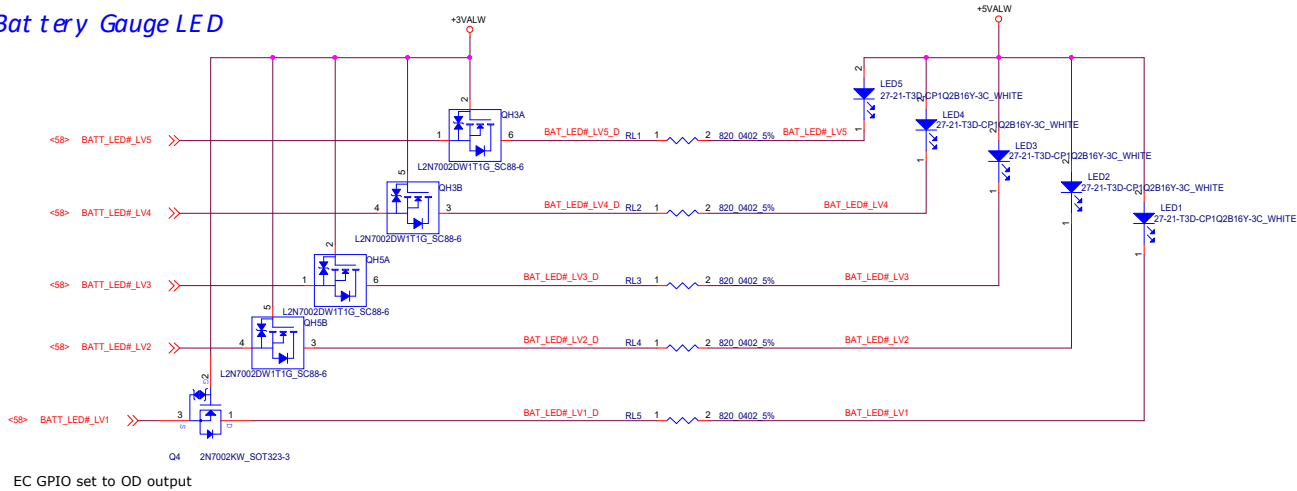
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BATT LED Power Button



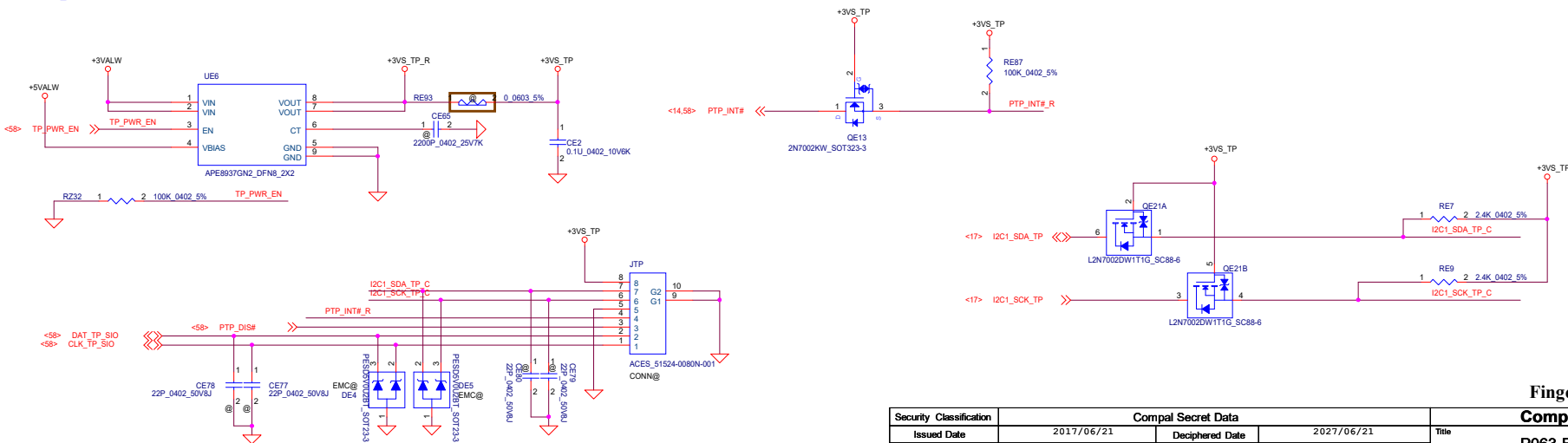
Battery Gauge LED



Power Button and LED



Touch pad



Fingerprint Reader CONN

Compal Electronics, Inc.

P063-BAT LED/TP/SW

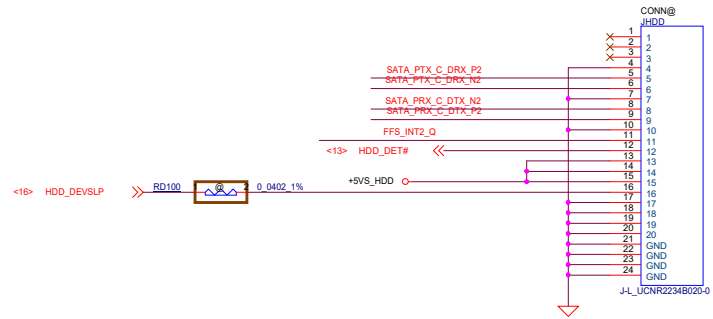
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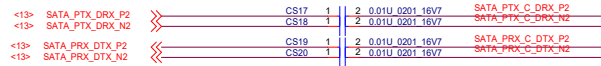
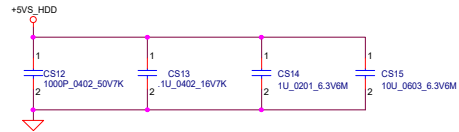


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HDD CONN

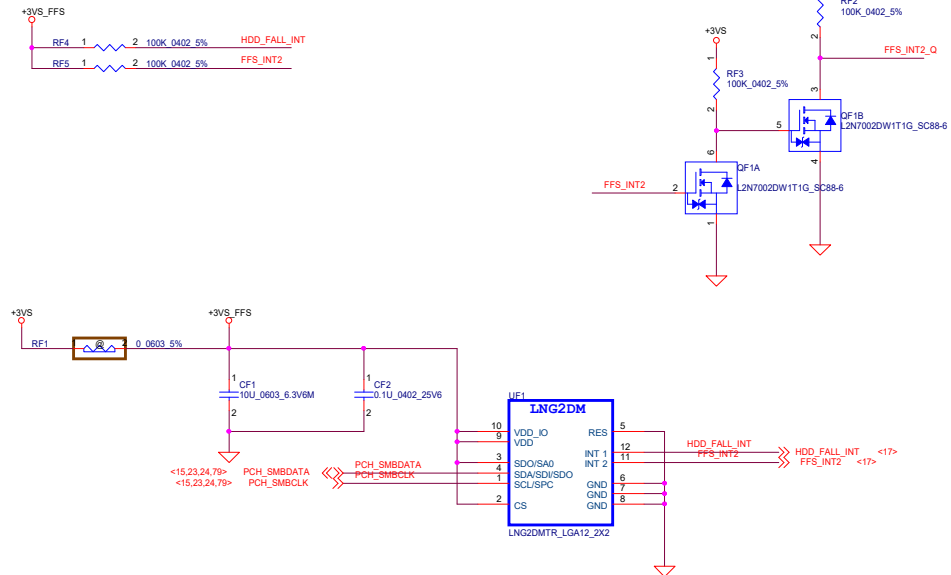


Place near HDD CONN (JHDD1)



BYPASS Circuit

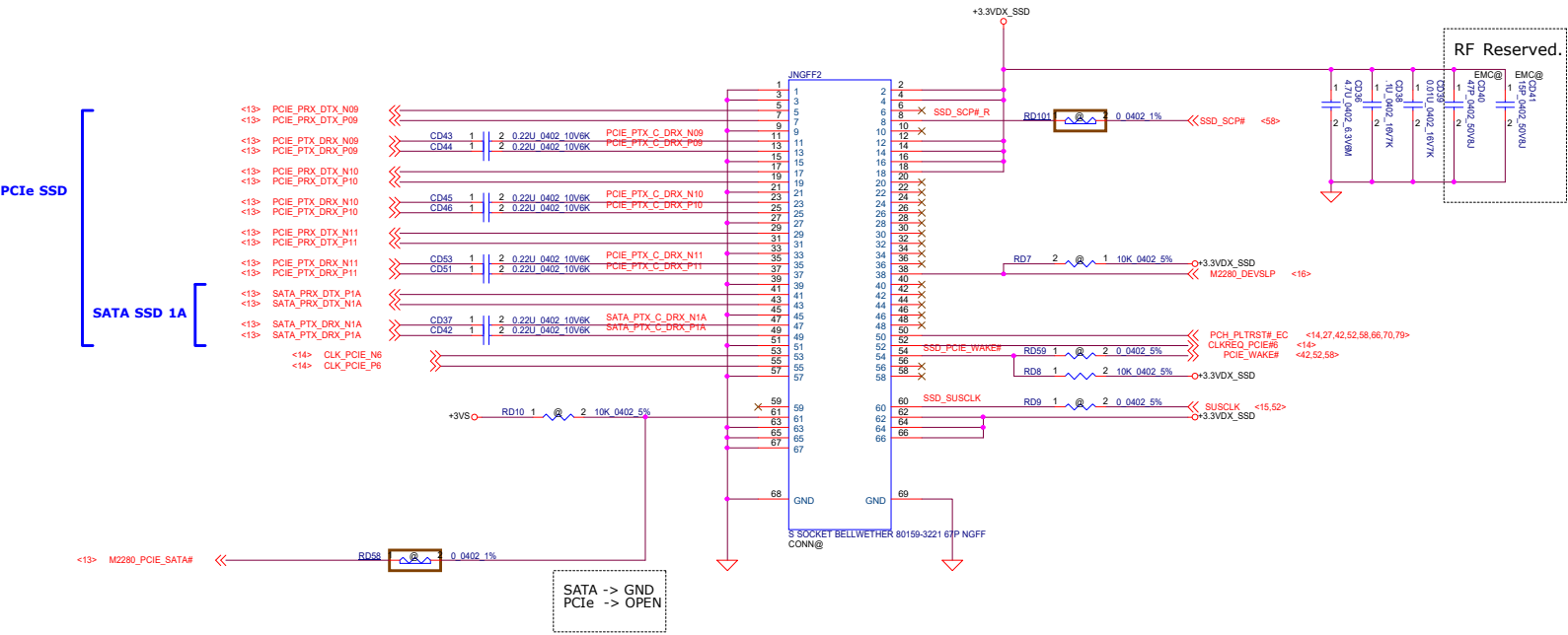
Free Fall Sensor



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M.2 Slot-C Key-M (SSD)

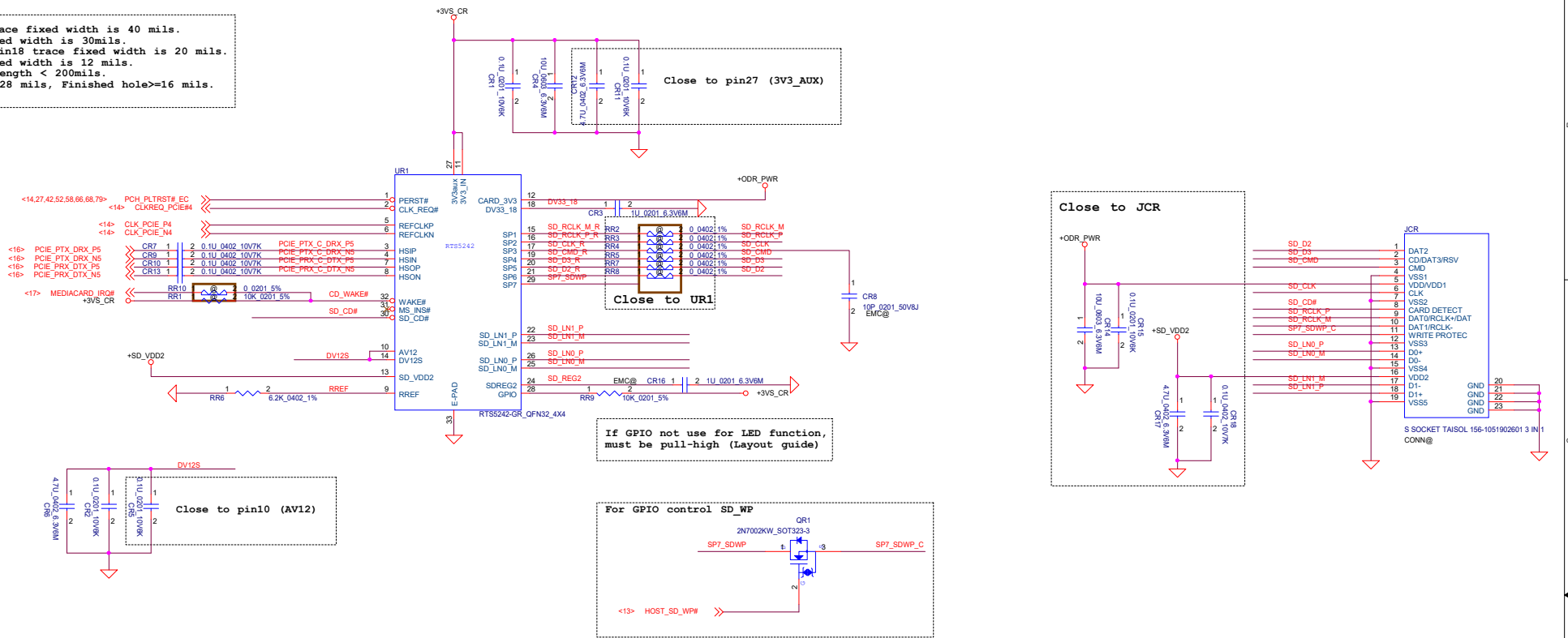




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Card Reader

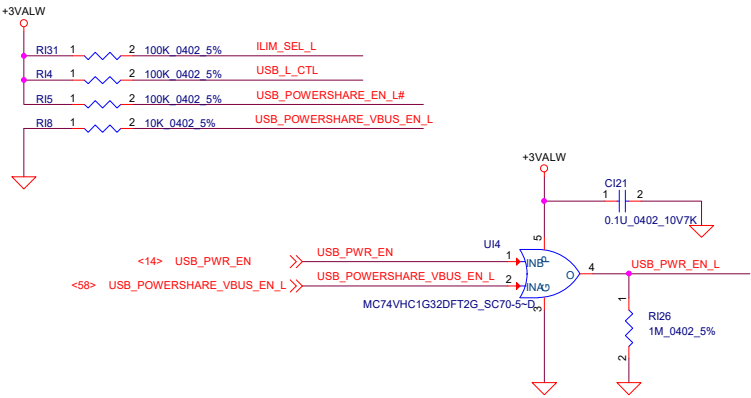
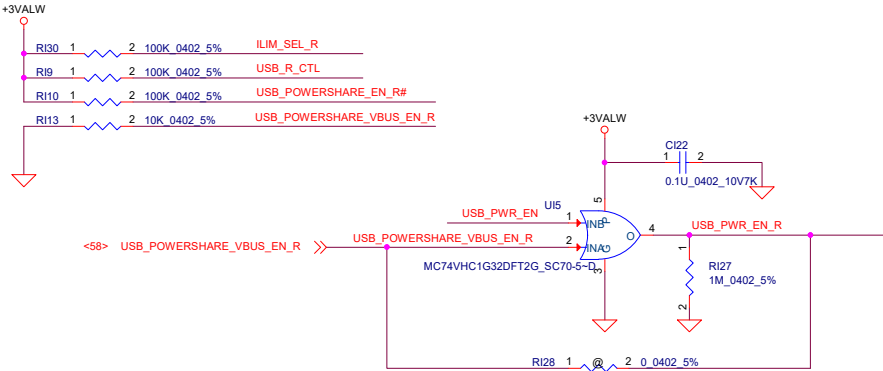
Pin11, Pin12 trace fixed width is 40 mils.
Pin27 trace fixed width is 30mils.
Pin10, pin14, pin18 trace fixed width is 20 mils.
Pin 9 trace fixed width is 12 mils.
Trace routing length < 200mils.
Via size: Pad>=26 mils, Finished hole>=16 mils.



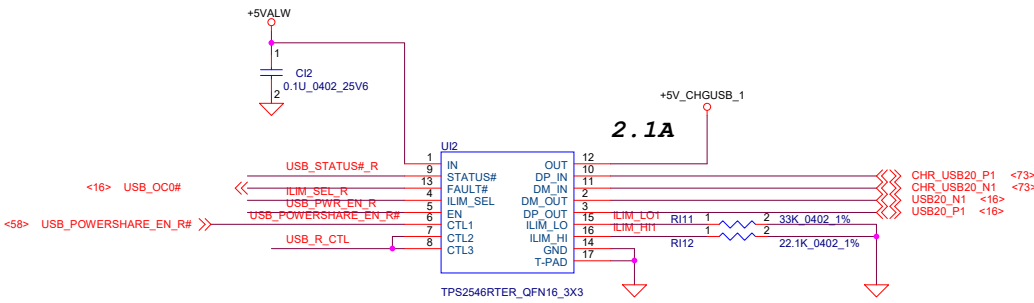
USB Powershare

Device Control Pins				Flow Line Condition
CTL1	CTL2	CTL3	ILIM_SEL	
0	1	1	X	DCP AUTO
1	1	1	0	SDP
1	1	1	1	CDP

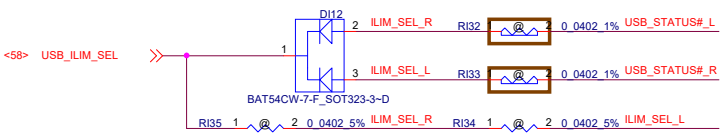
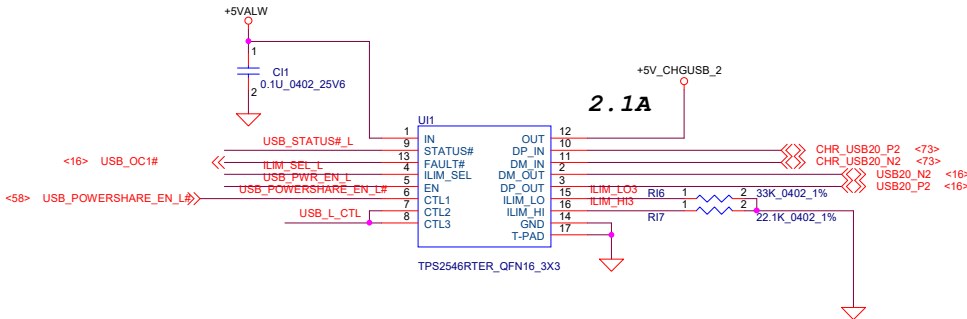
Suspend mode	CTL1 = 0 : Enable Power Share DCP mode in Suspend mode
	CTL1 = 1 : Disable Power Share in Suspend mode (For Support USB wake)
S0 mode	ILIM_SEL = 0 : SDP mode (0.9A by ILIM_LO setting)
	ILIM_SEL = 1 : CDP mode (STATUS# trigger by ILIM_HI =2.2A)

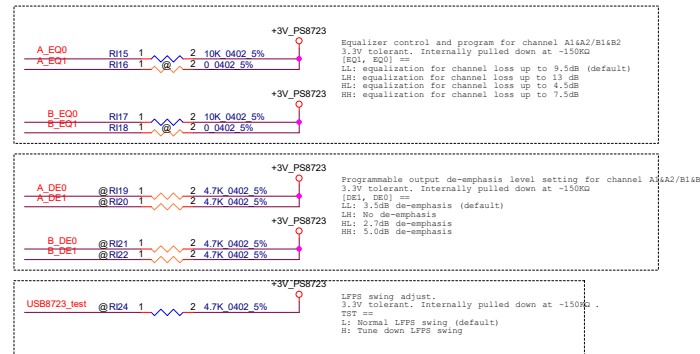


USB3.1 / USB2.0 Port1 (Right Side)

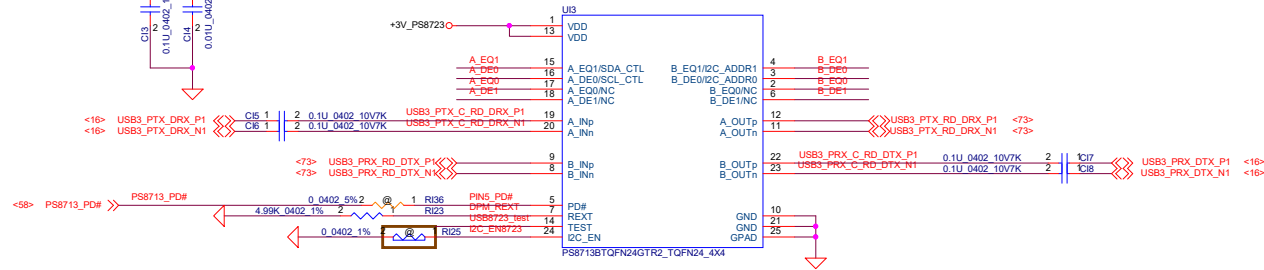


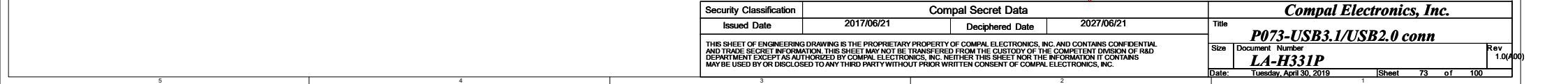
USB3.1 / USB2.0 Port2 (Left Side)





USB3.0 Re-driver





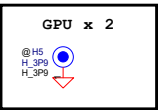
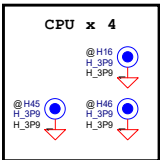


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				P074-Reserve	
				Size	Document Number
				LA-H331P	
Date:		Tuesday, April 30, 2019		Sheet	74 of 100
3		1	2	Rev 1.0(A00)	

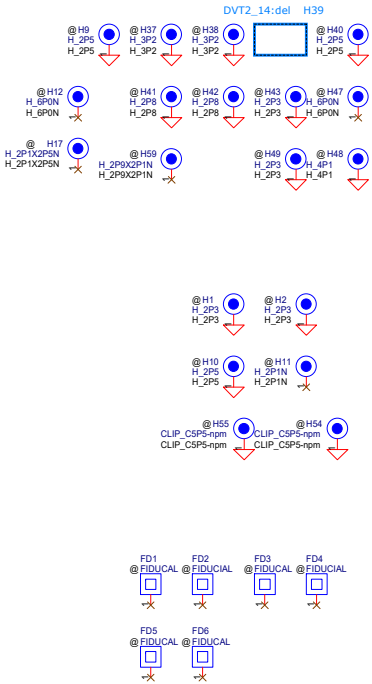
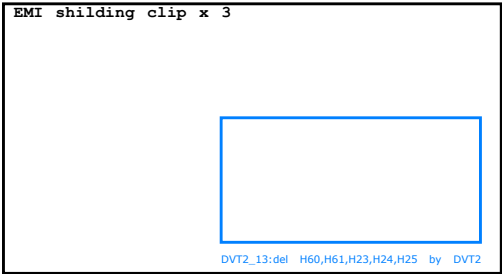
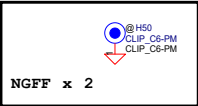


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				P075-Reserve	
				Size	Document Number
				LA-H331P	
Date:		Tuesday, April 30, 2019		Sheet	75 of 100
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Screw Hole



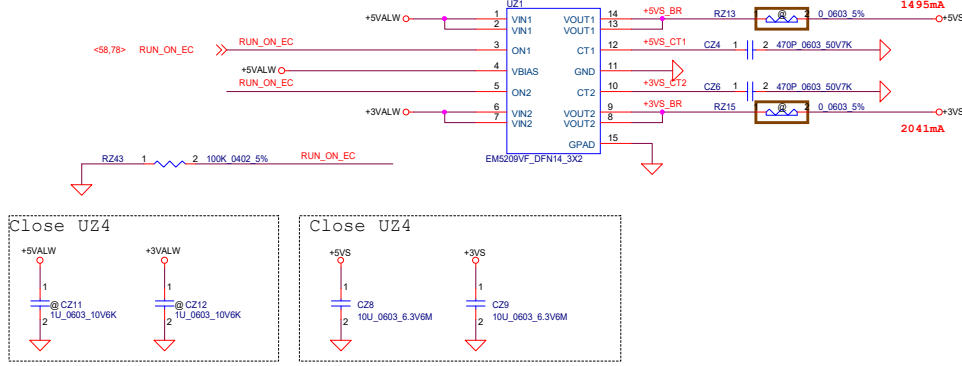
X03 1222: for peel off issue, change footprint to CLIP_C6-PM



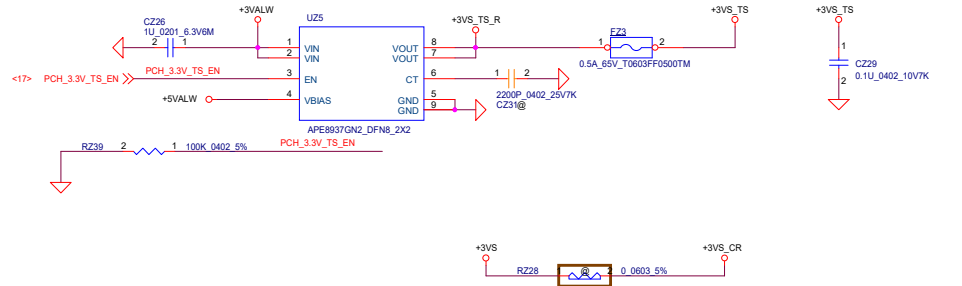
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Size	Document Number			Rev	1.0/100
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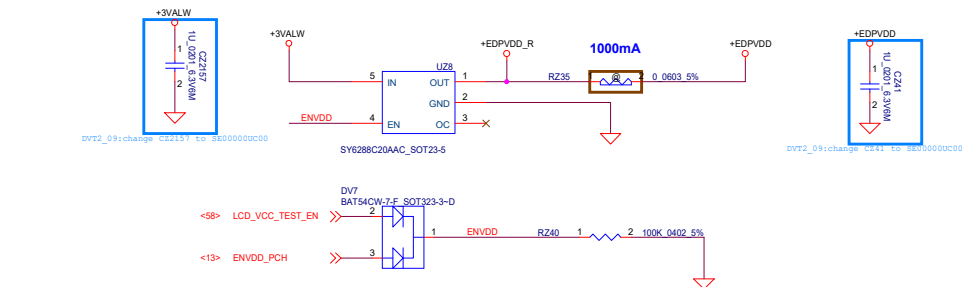
+5VALW to +5VS
+3VALW to +3VS



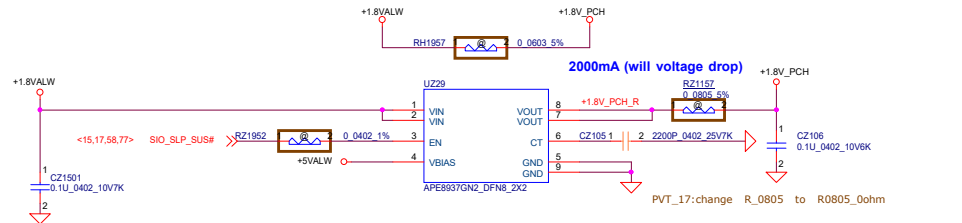
Touch Screen Load Switch & Card Reader



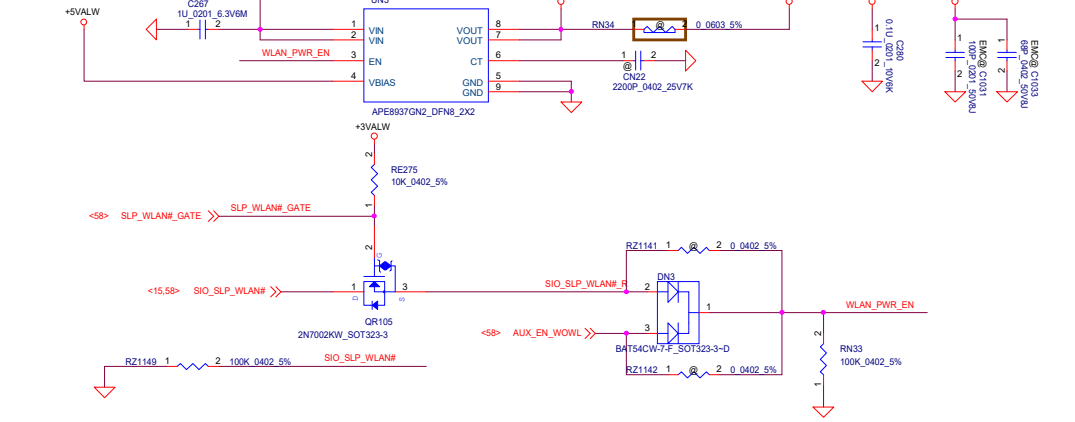
eDP & Camera Load Switch



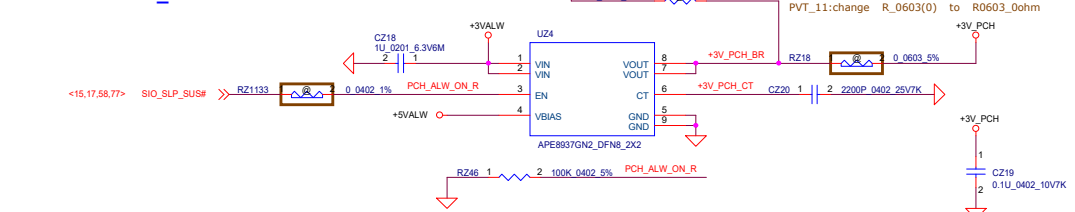
+1.8VALW to +1.8V_PCH



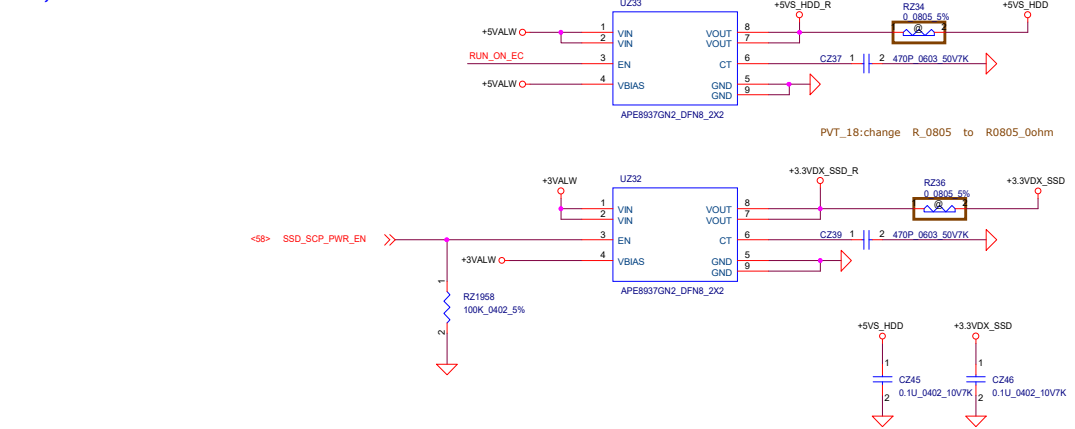
WLAN Load Switch



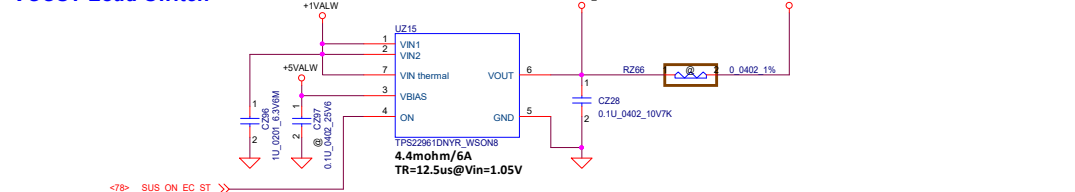
+3VALW to +3V_PCH



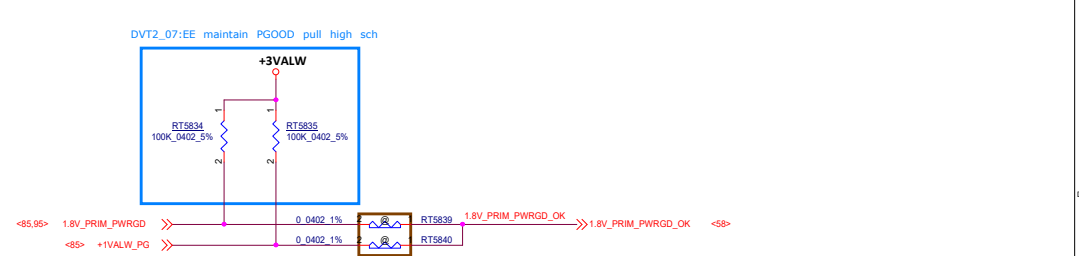
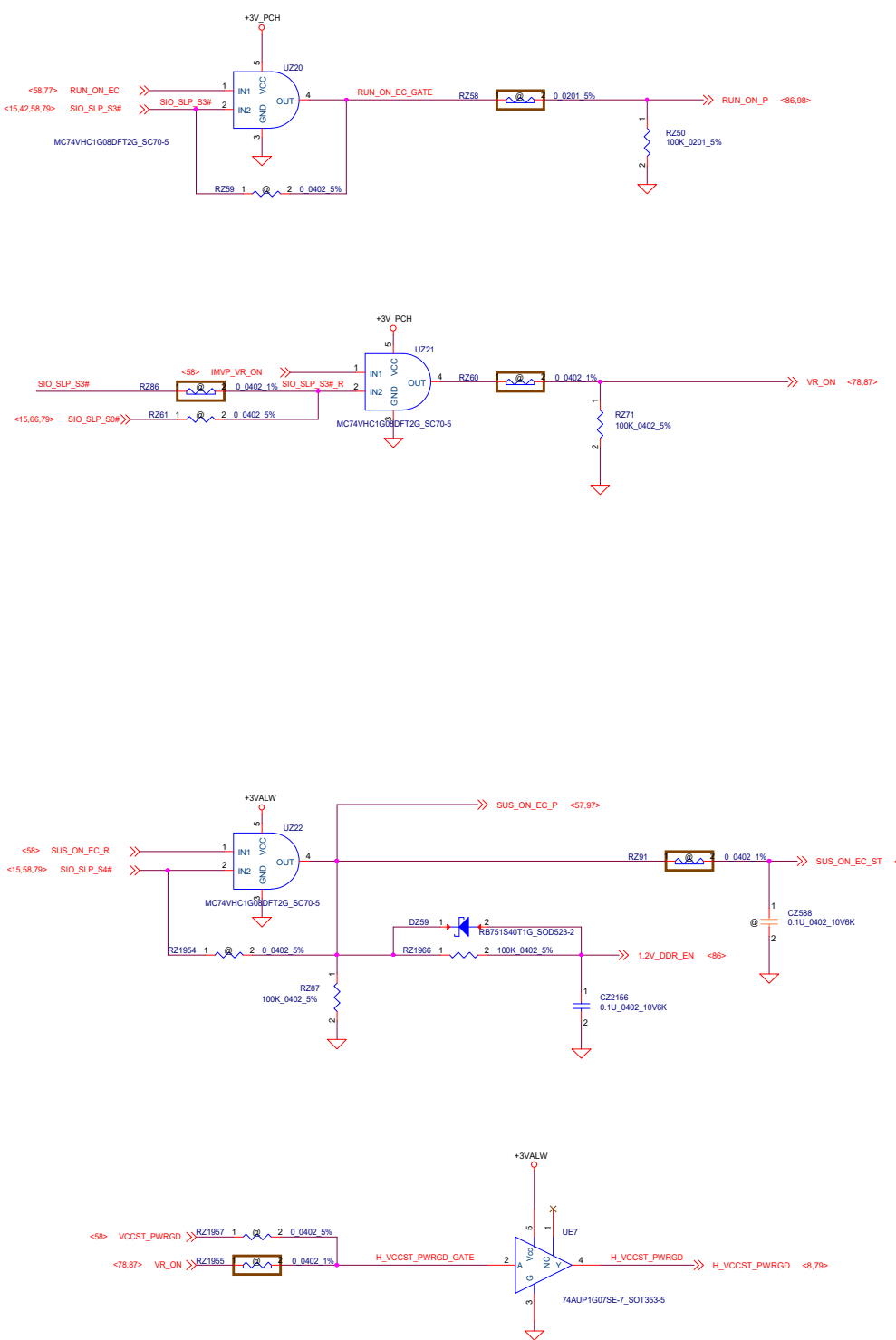
HDD, SSD Load Switch



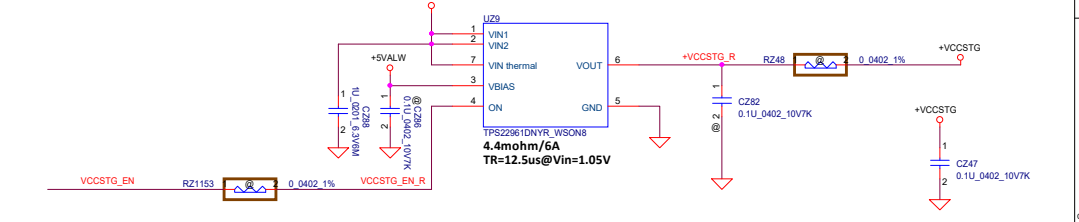
+VCCST Load Switch



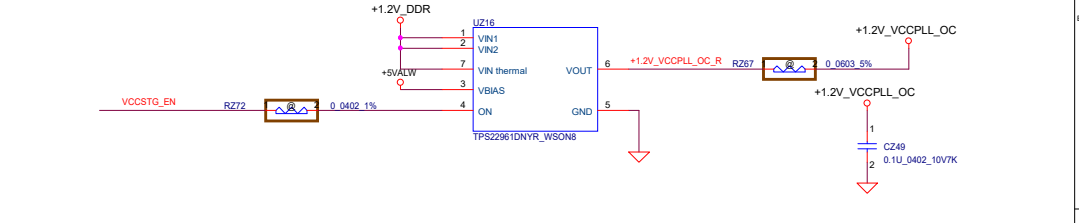
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Document Number				LA-H331P
Date:				Tuesday, April 30, 2019



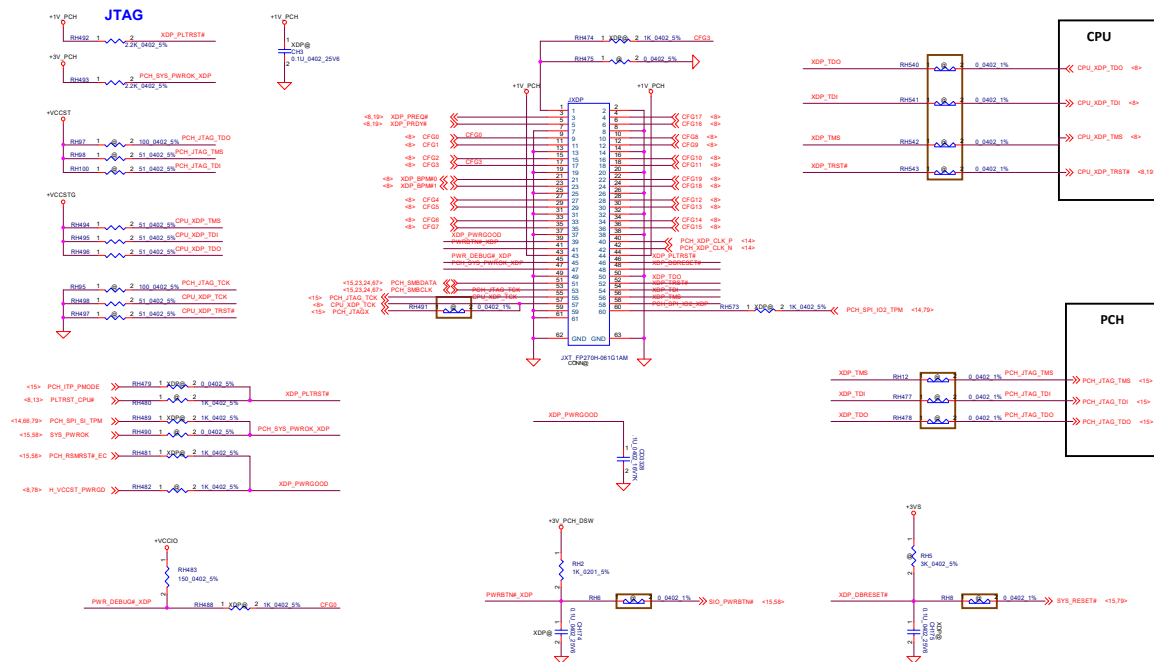
+VCCSTG Load Switch



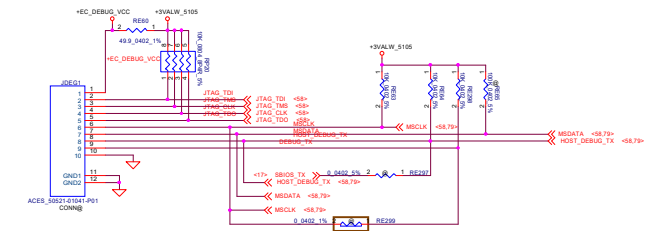
+VCCPLL_OC Load Switch



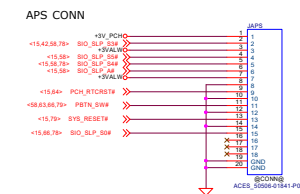
JXDP



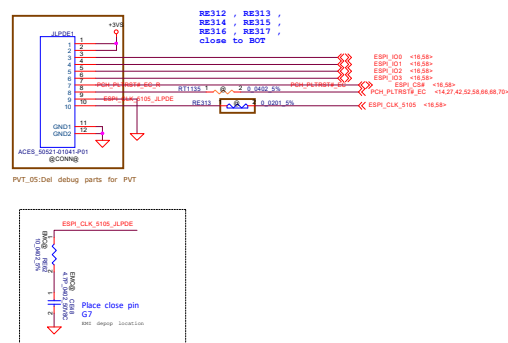
JDEG



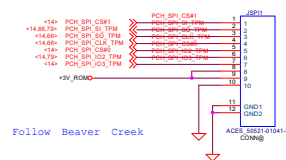
JAPS



JLPDE

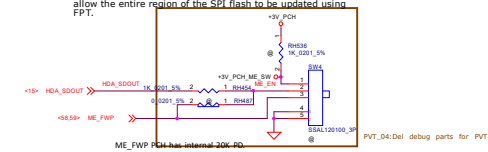


JSPI



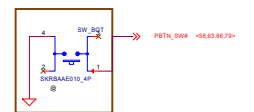
ME LOCK SW

Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.



ME_FWP PCH has internal 20K PD

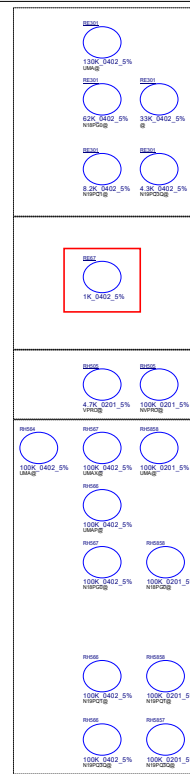
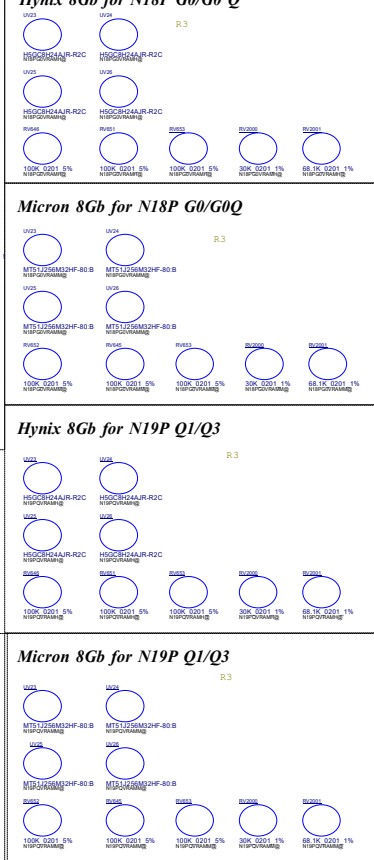
(not be updated) ----> Pin1 & Pin2 short
 (not be updated)-->Pin3 & Pin2 short(Default



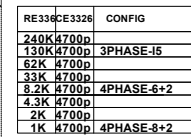
PVT_05:Del debug parts for PVT

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			P078-XDP/APS/SP/L/PDF...Debug	
			Date	
			14/04/2017	
			Version	
			1	
			Total	
			1	
			Page	
			1	
			Total	
			1	

Hynix 8Gb for N18P G0/G0 Q

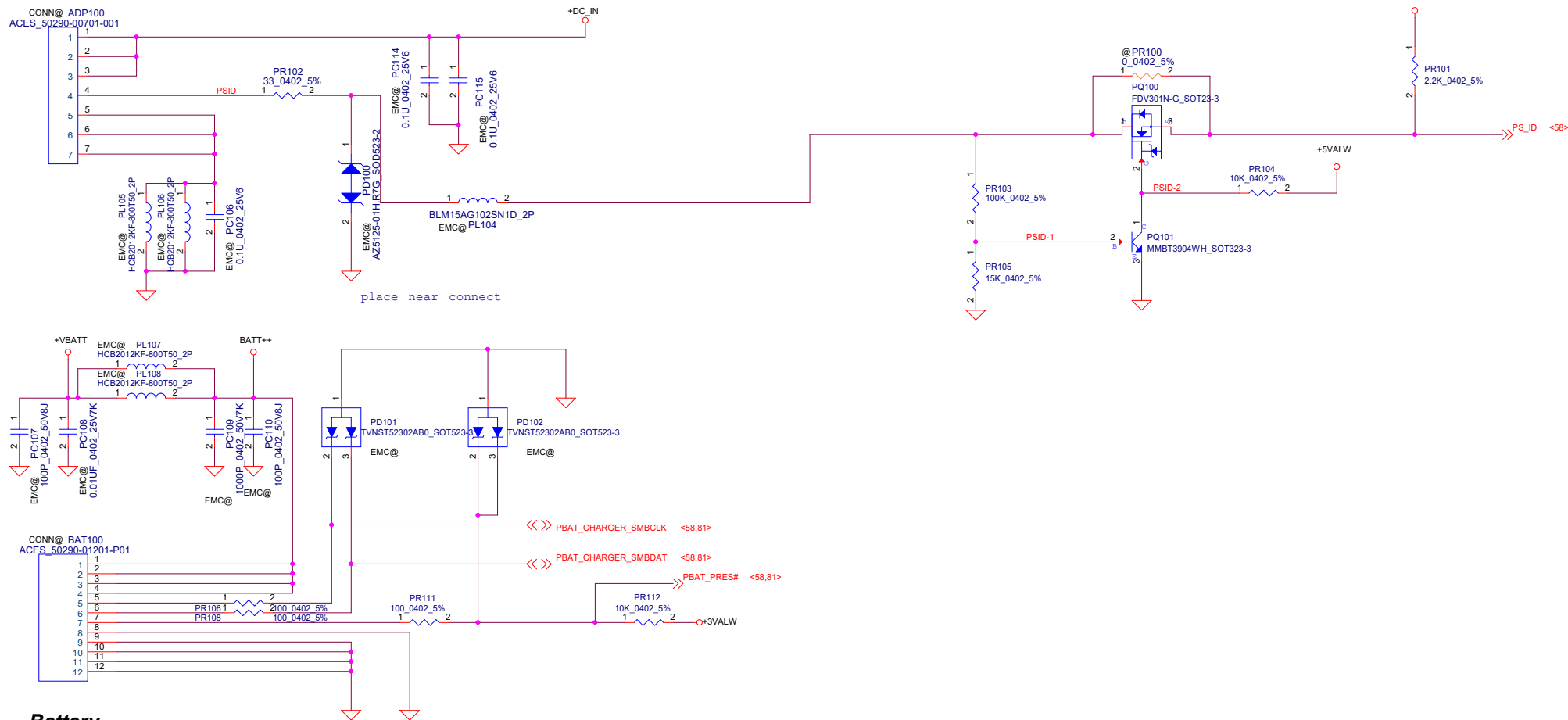


TLS CONFIDENTIALITY	
HIGH(4.7K)	
LOW(DEFAULT)(100K)	
BIOS 20k internal pull-down	



GPU type	Config Sku/Division		SYSTEM ID1	SYSTEM ID2		SYSTEM ID3
			BID ID3	BID XPS	C5MB / BID Per	BID PC
IGFX	XPS C5MB	UMA	H	L	L	L
	Perision_BC	UMA	H	H	L	L
DGEFX	XPS C5MB	Nvidia N18P-G0	L	L	L	L
		Nvidia N18P-G0 MAX-Q	L	L	L	H
	Perision_BC	Nvidia N19P-Q1	L	H	L	L
		Nvidia N19P-Q3 MAX-Q	L	H	H	H

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Smart Adapter circuit (39.1)

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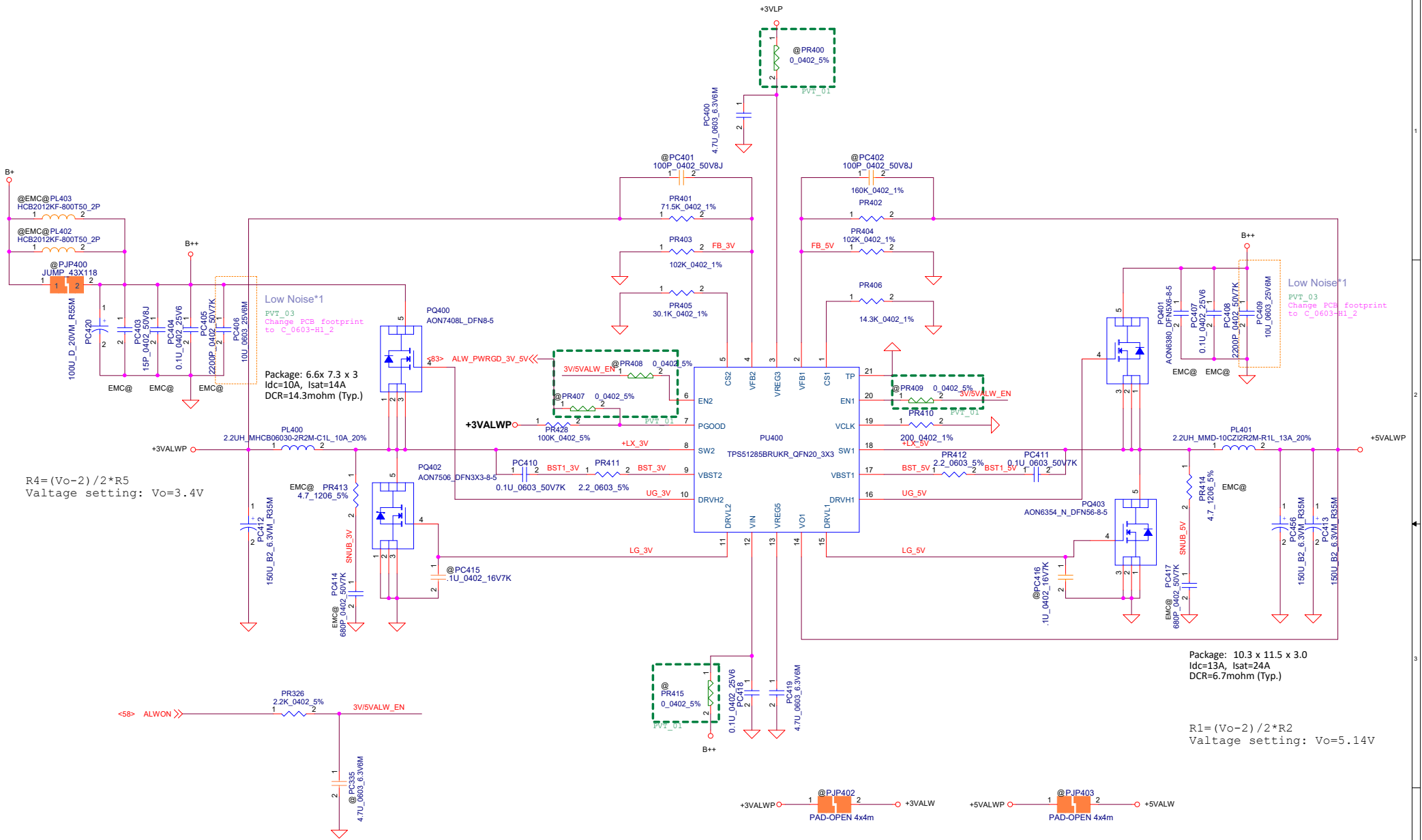
Compal Electronics, Inc.

Title
P082-PWR_DCIN / BATT CONN / OTP

Size
Document Number
LA-H331P

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0.1(00)

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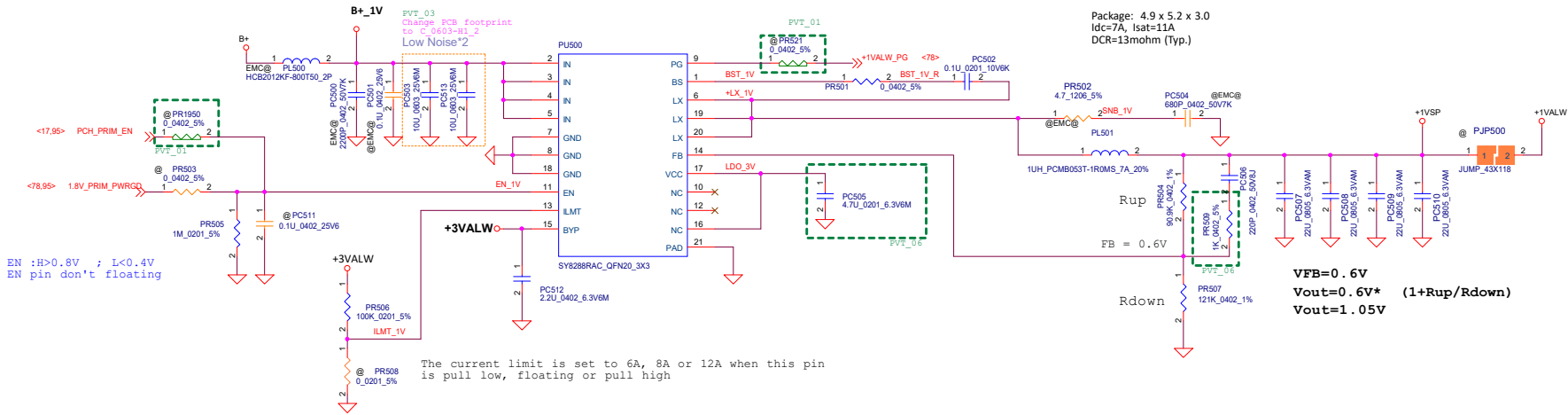
3V/5V controller(35.1), Support component(35.2)

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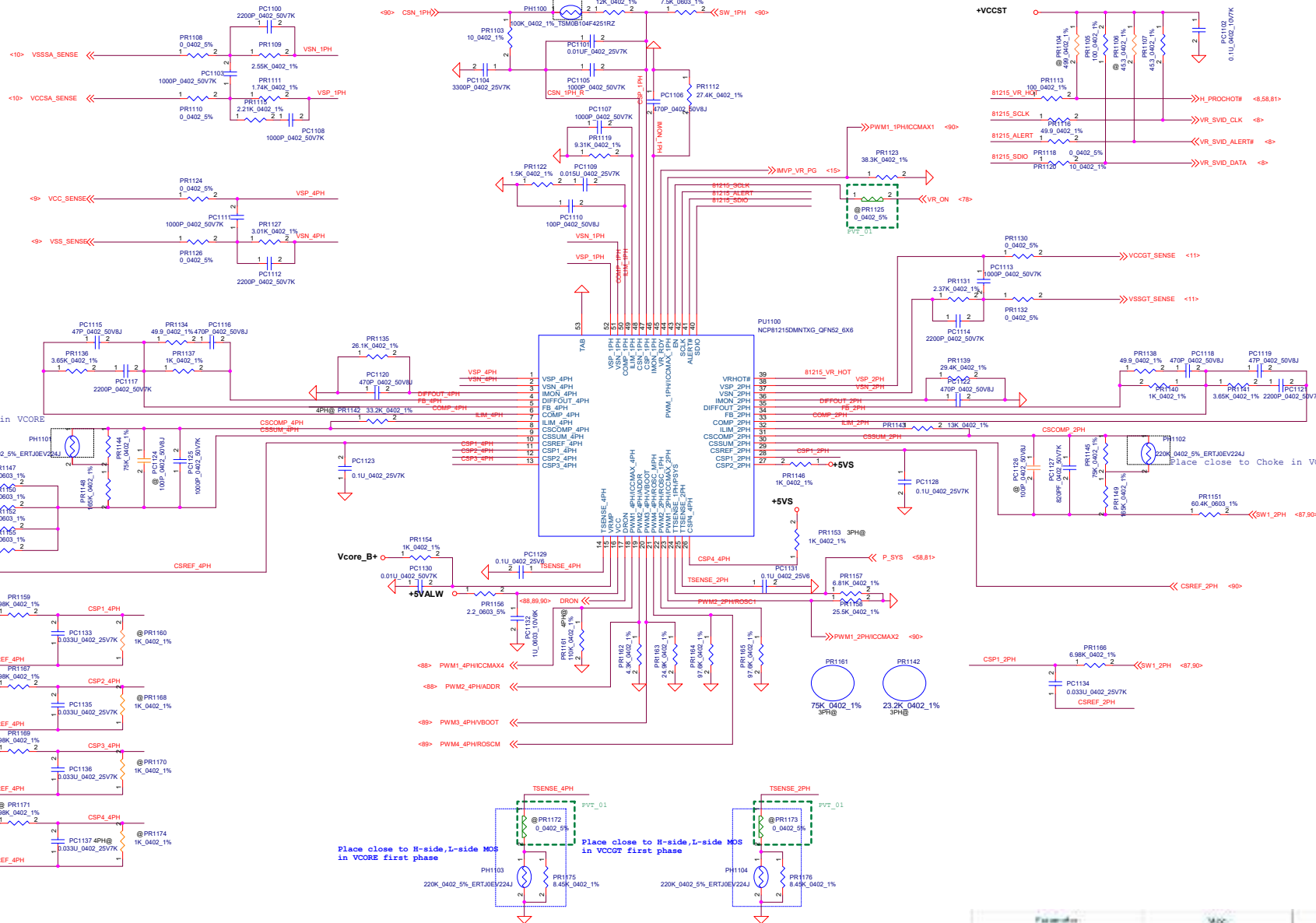
Compal Electronics, Inc.			
Title		P084-PWR 3.3VALWP/5VALWP	
Size	Document Number	LA-H331P	
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+1VSP
TDC 6.3A
Peak Current 9A
OCP current 12A(fix)



PWR.Plane.Regulator(35.5), Support component(35.6)

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Parameter	VOC	VOC _{ORG}	VOC _{CSA}
SPG (g)	25.0 (0.100)	25.0	30.0
Deformation (mm)	5.0 in the PG and 6.0 in the others		

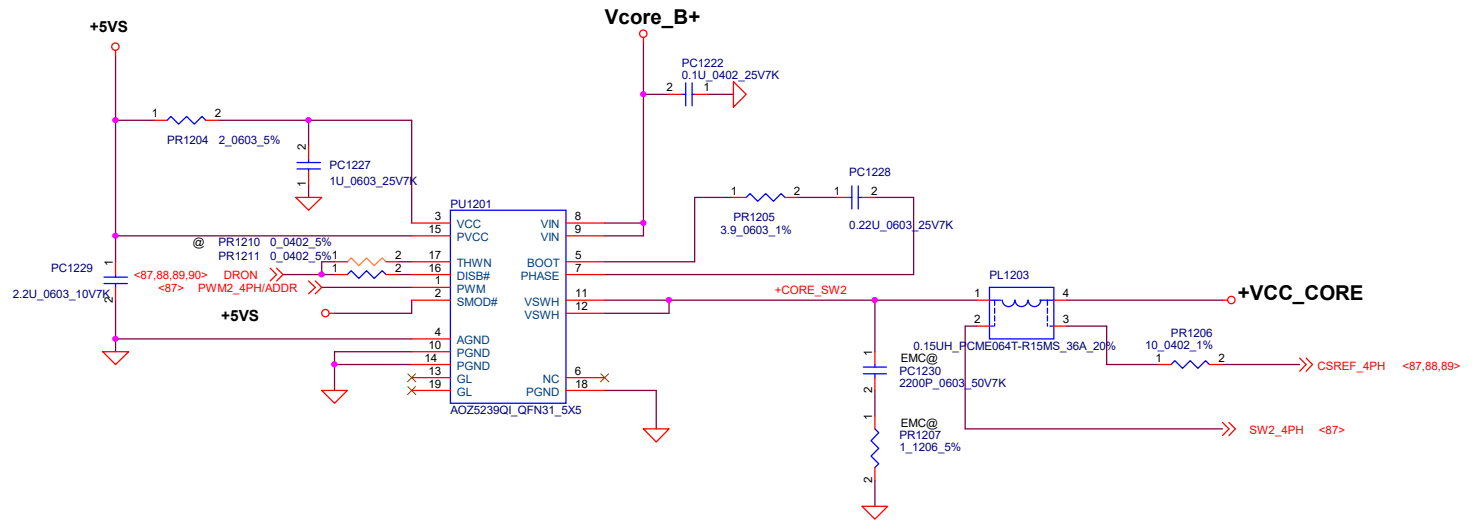
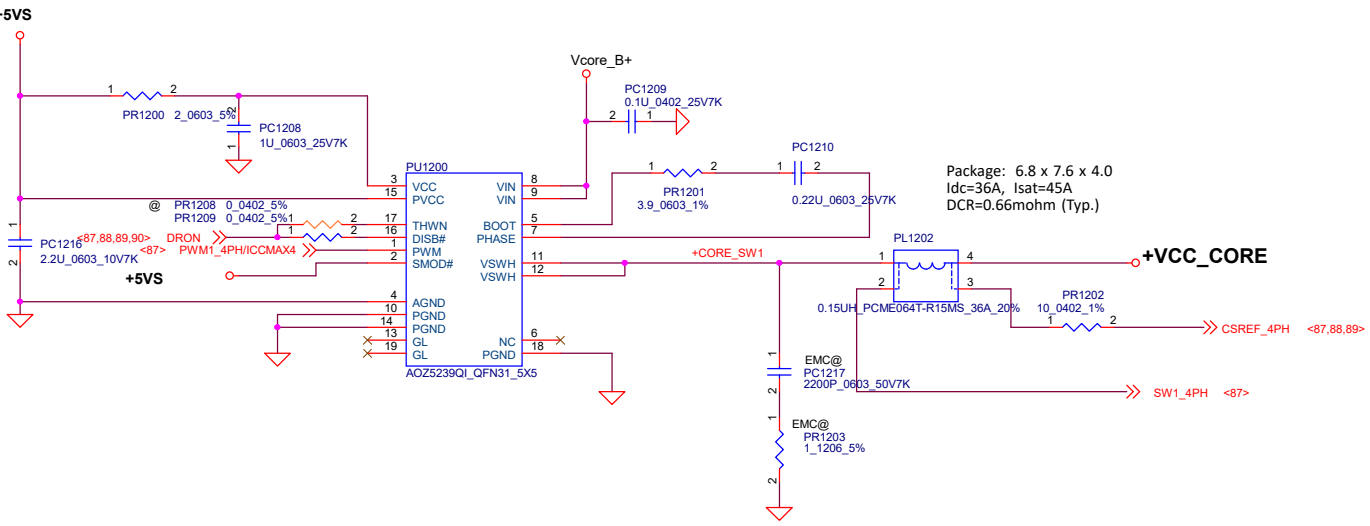
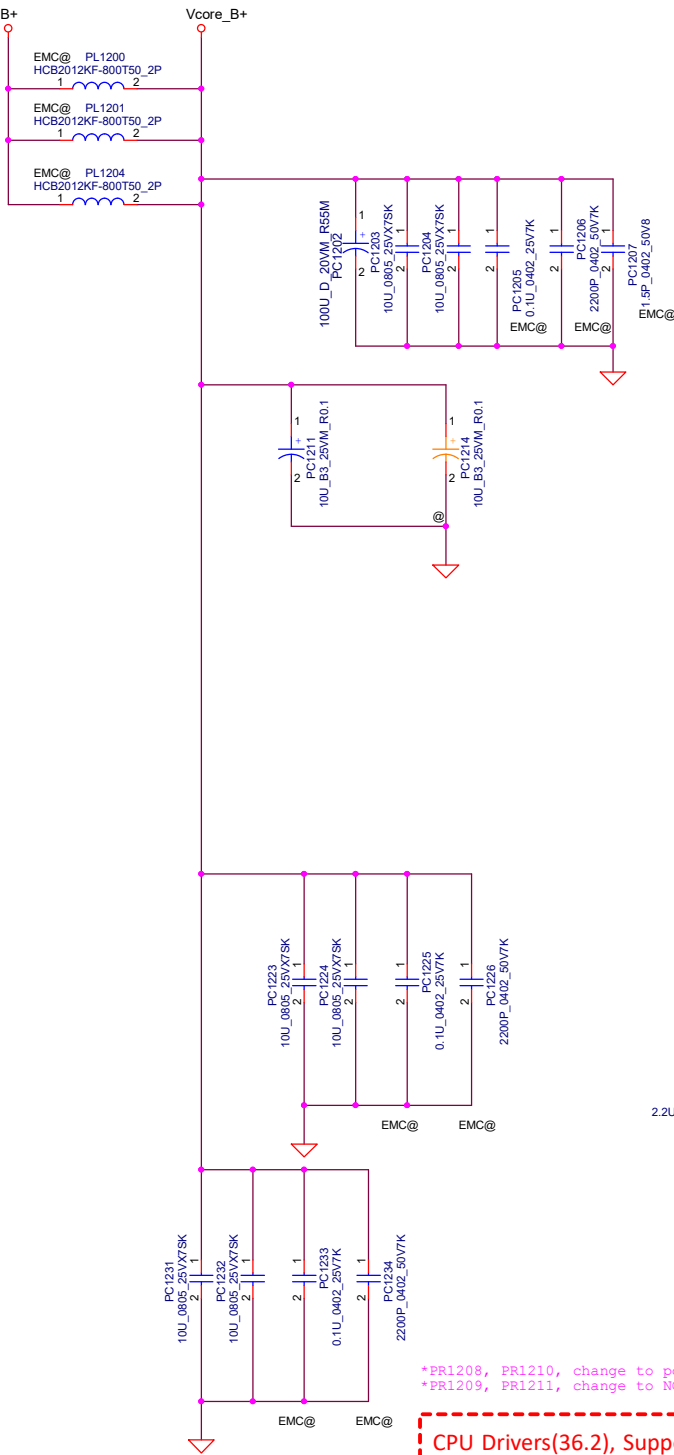
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CPU control PWM IC(36.1), Support component(36.3)

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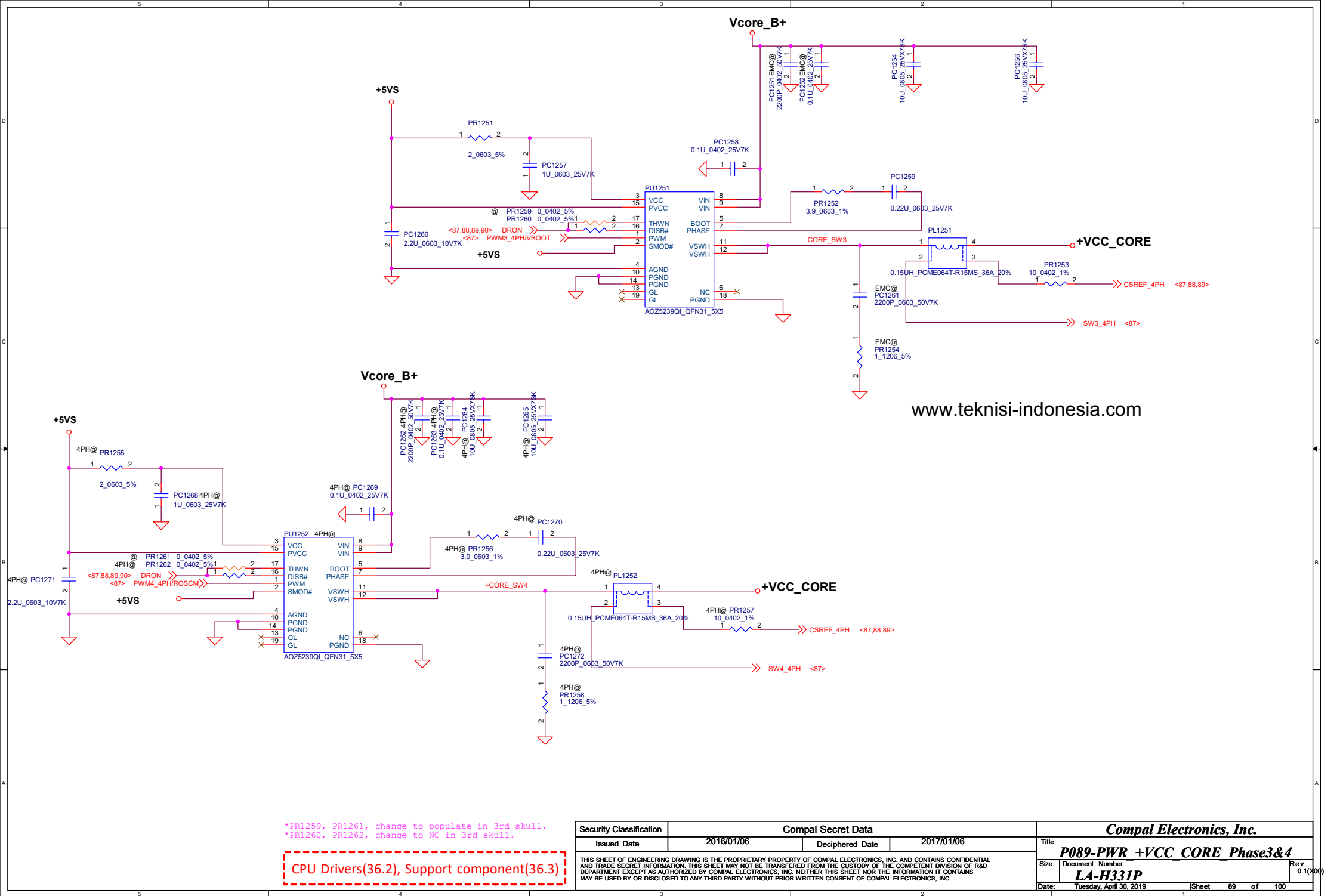


*PR1208, PR1210, change to populate in 3rd skull.
*PR1209, PR1211, change to NC in 3rd skull.

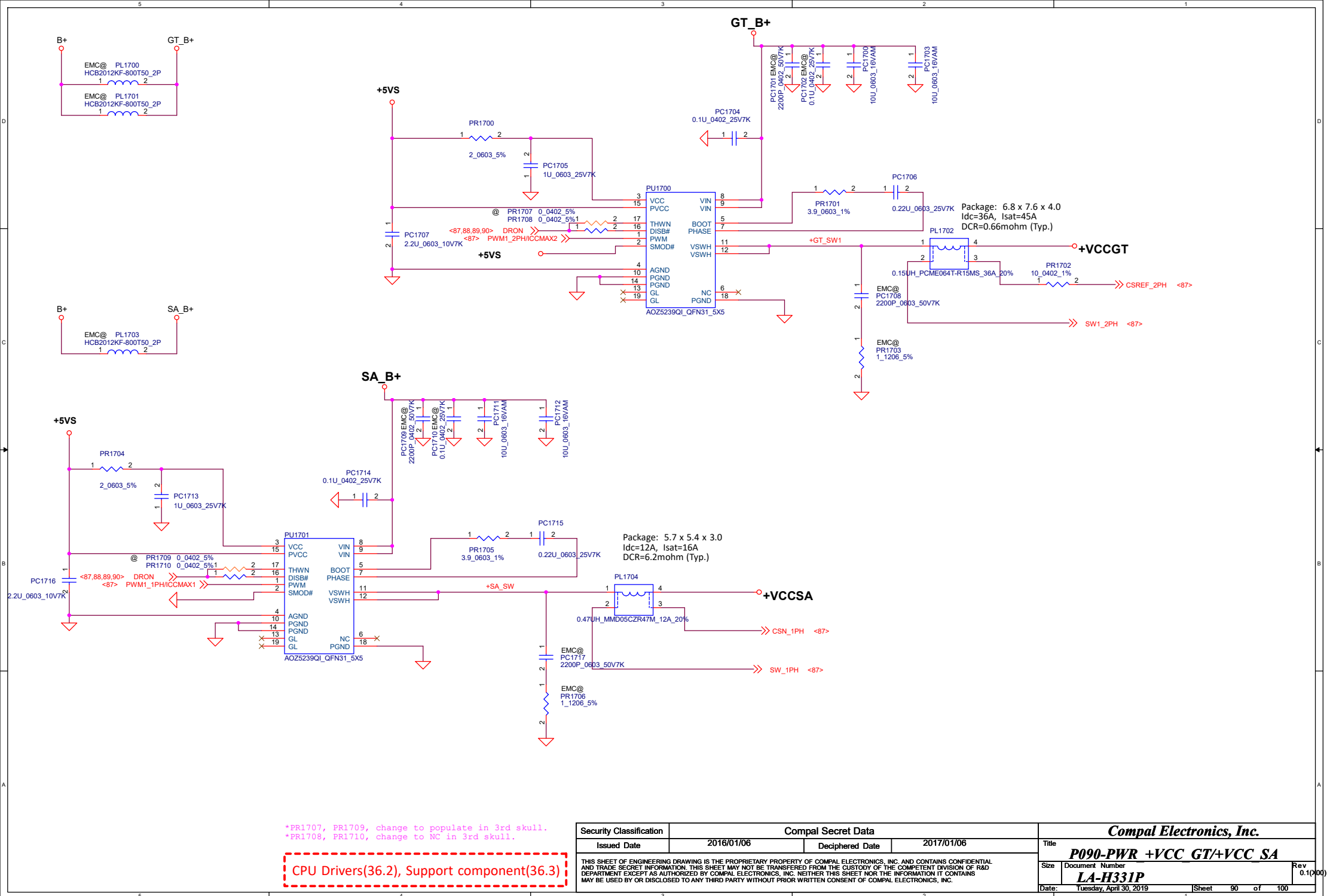
CPU Drivers(36.2), Support component(36.3)

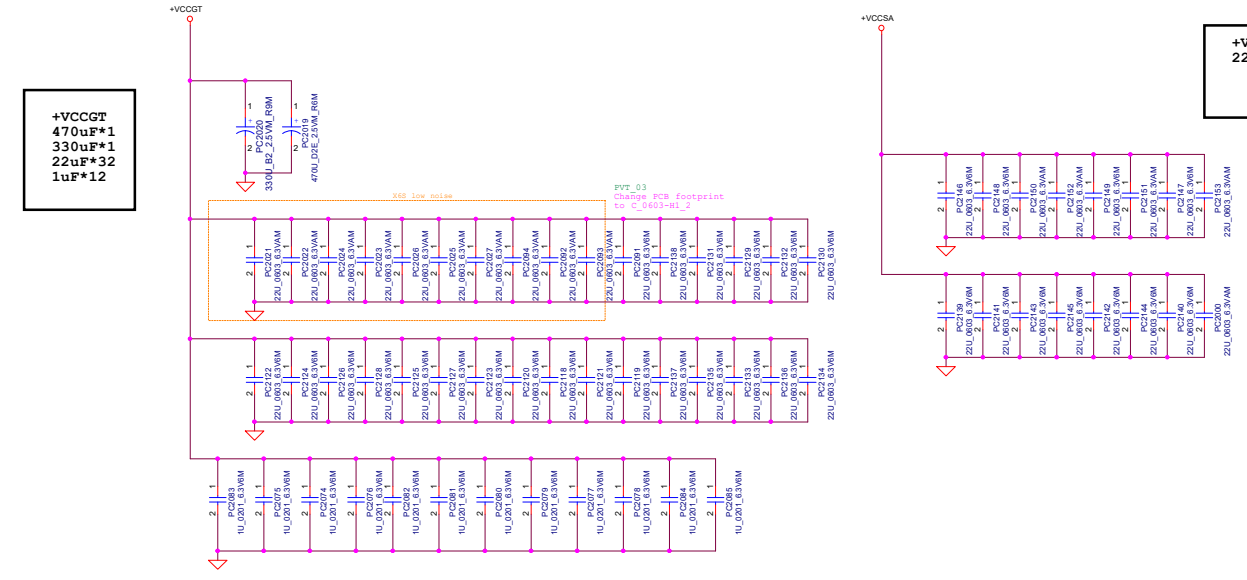
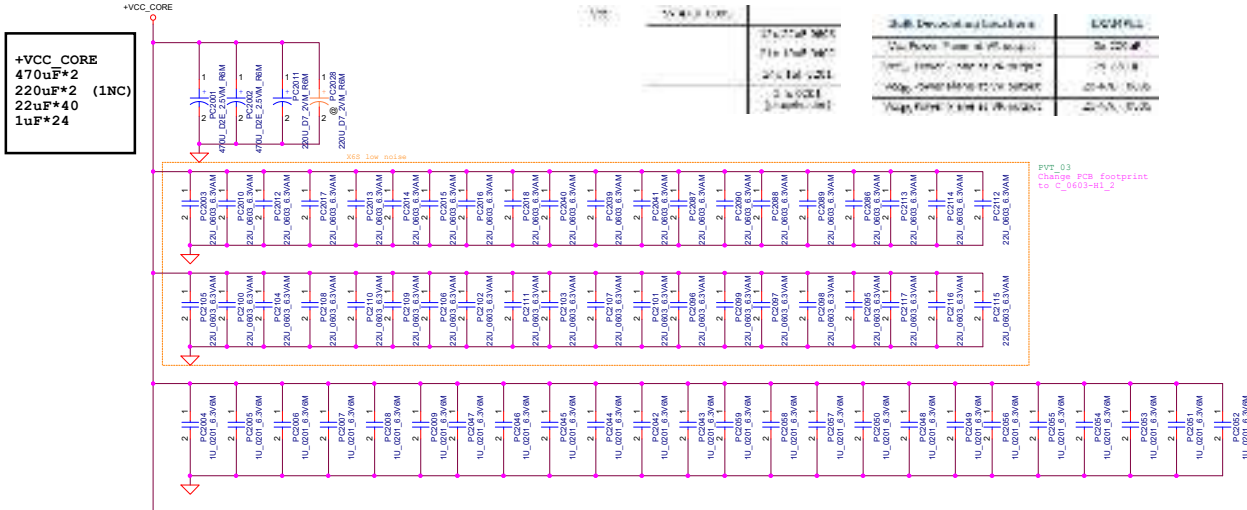
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								P088-PWR +VCC CORE Phase1&2	
Size		Document Number						Rev 0.1(000)	
LA-H331P									
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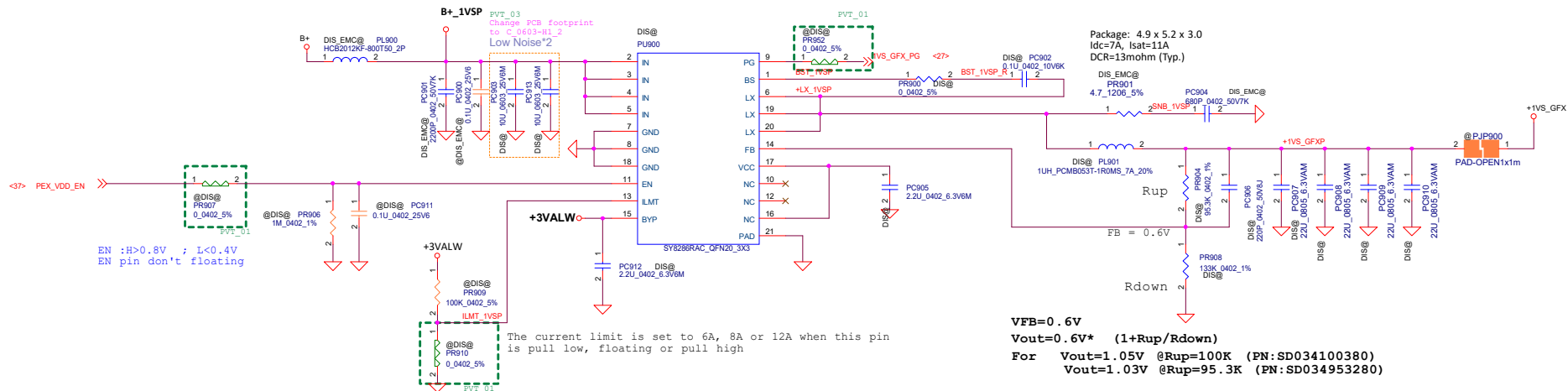


CPU Output CAPS(36.4)

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				Date	Tuesday, April 30, 2019
				Sheet	91 of 100

for dGPU SKU
@DIS@ : Nopop Component
DIS@: POP for dGPU SKU

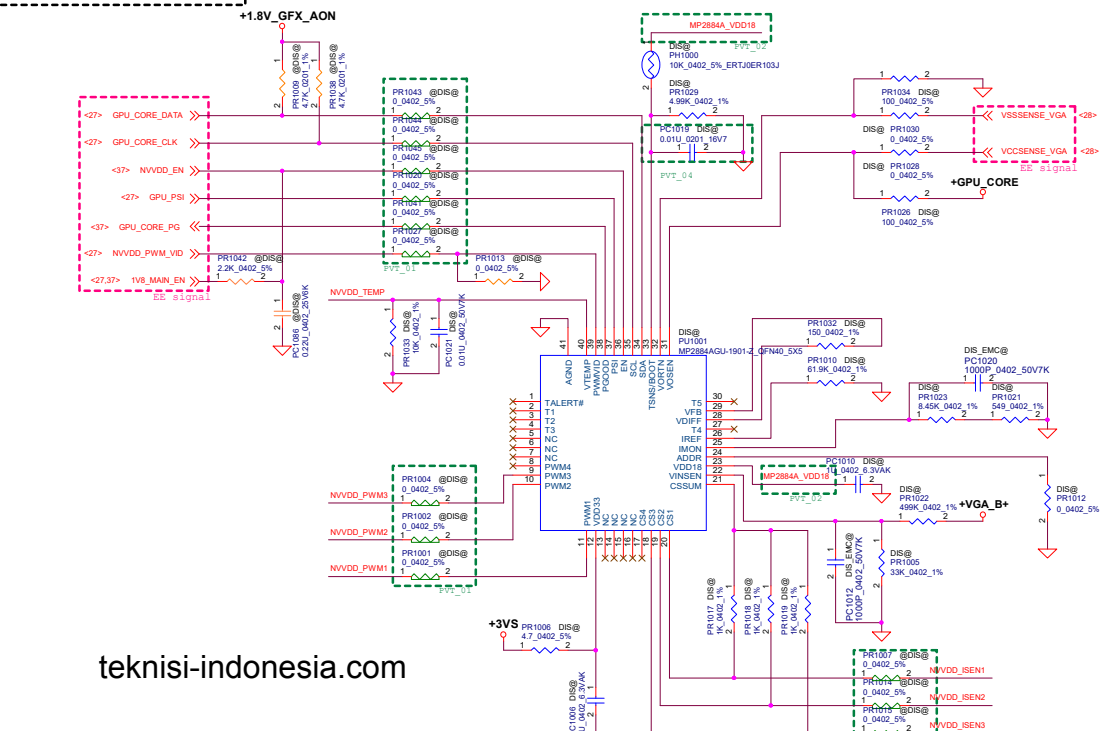
+1.0VSP/1.05VSP
TDC 1.1A
Peak Current 1.1A
OCP current 6A(fix)



GPU other power_Regulatorr(43.7), Support component(43.8)

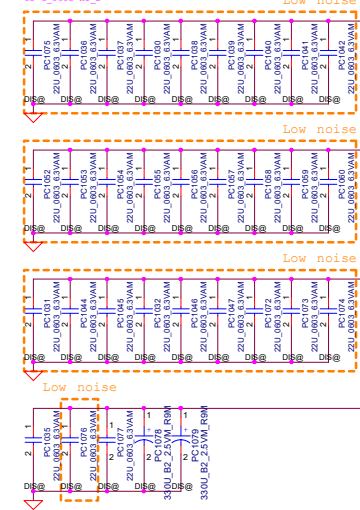
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for dGPU SKU
@DIS@ : Nopop Component
DIS@: POP for dGPU SKU



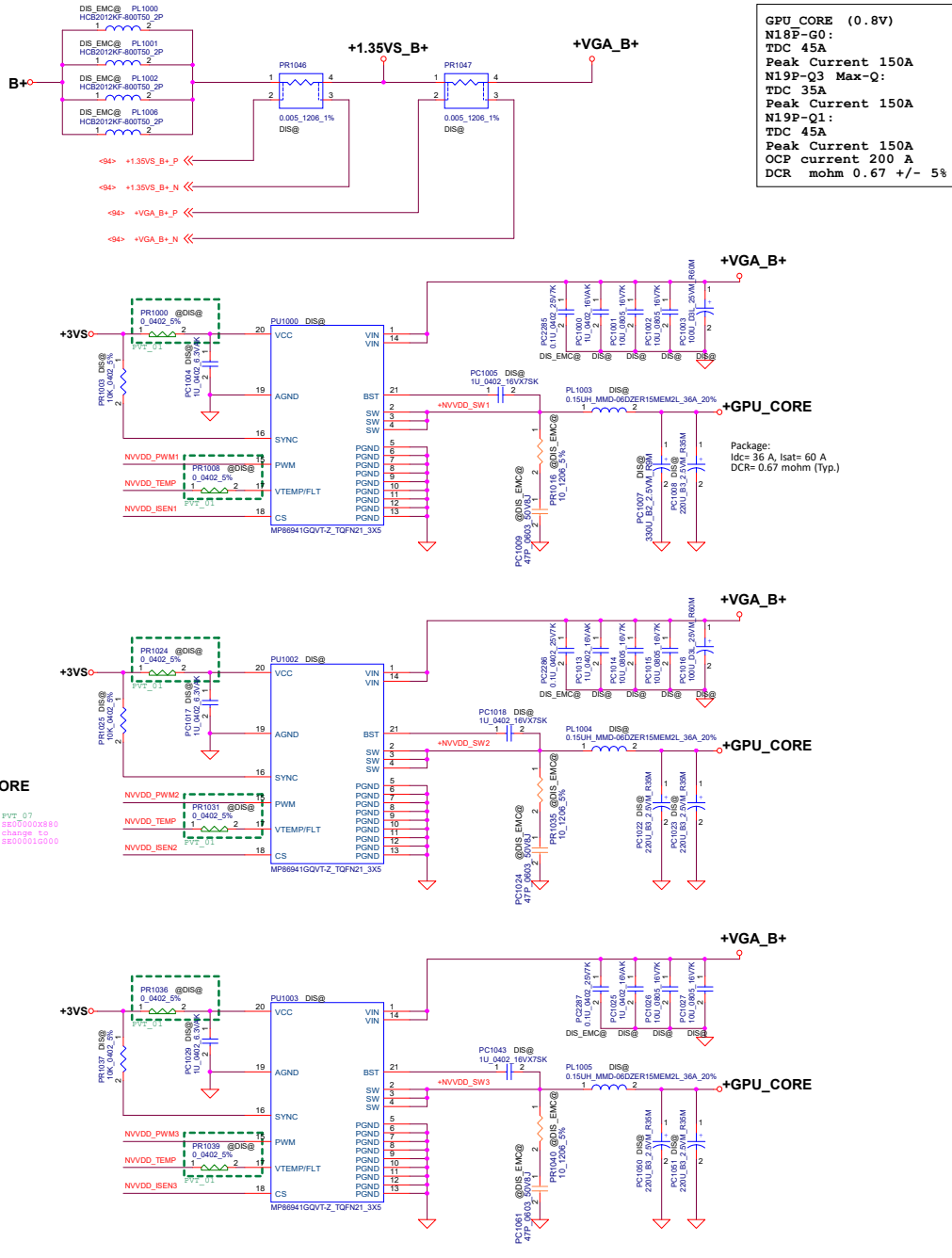
teknisi-indonesia.com

PVT_03
Change PCB footprint
to C_0603-W1_2




GPU_CORE
330uF*3
220uF*5
22uF*30
10uF*34
1uF*56 (25NC)

VGA_CORE controller(43.1), Support component(43.2)
VGA_CORE Drivers (43.3), GPU Core Output CAP (43.9)

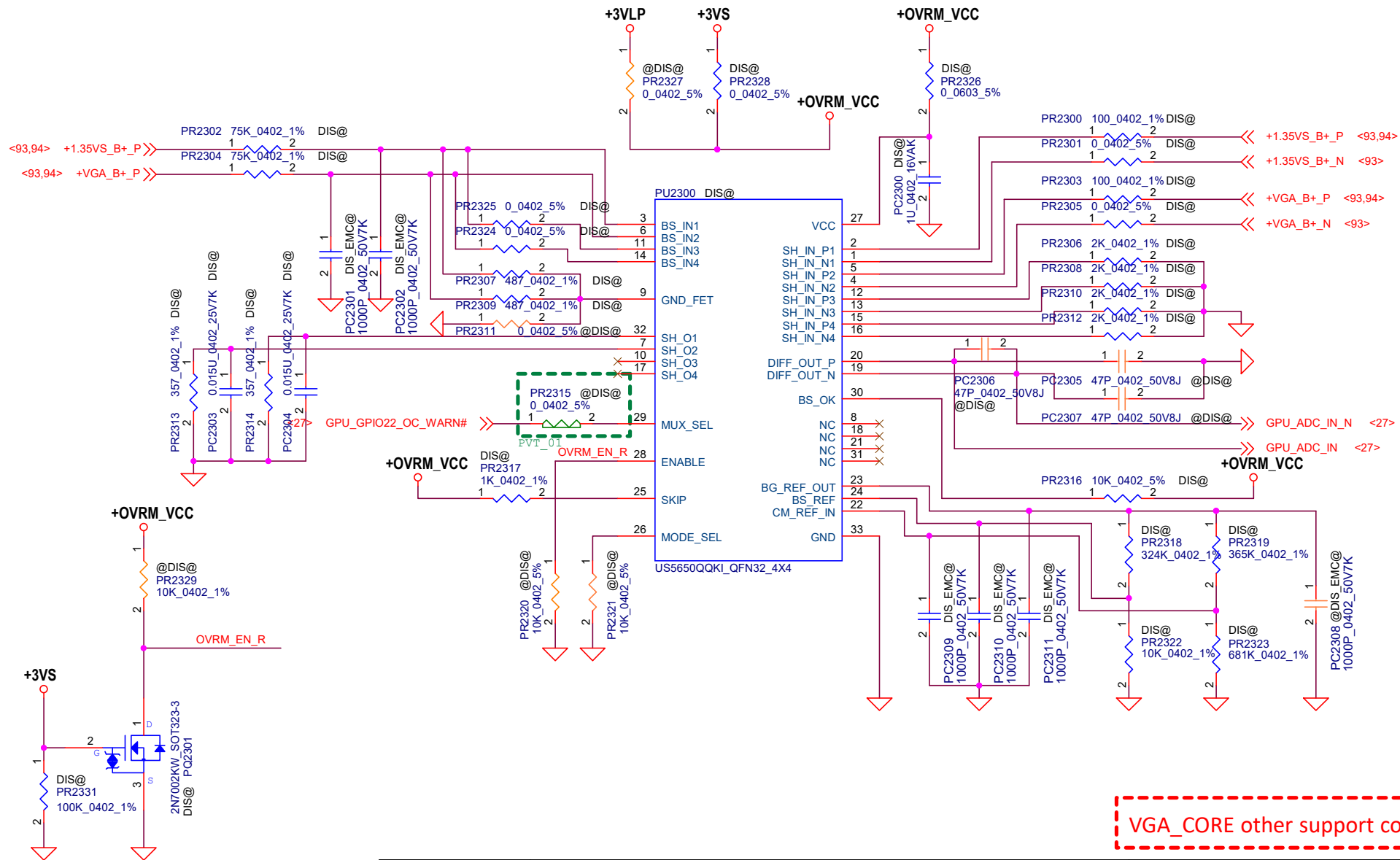


PVT_07
330uF*3
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22uF*30
10uF*34
1uF*56 (25NC)

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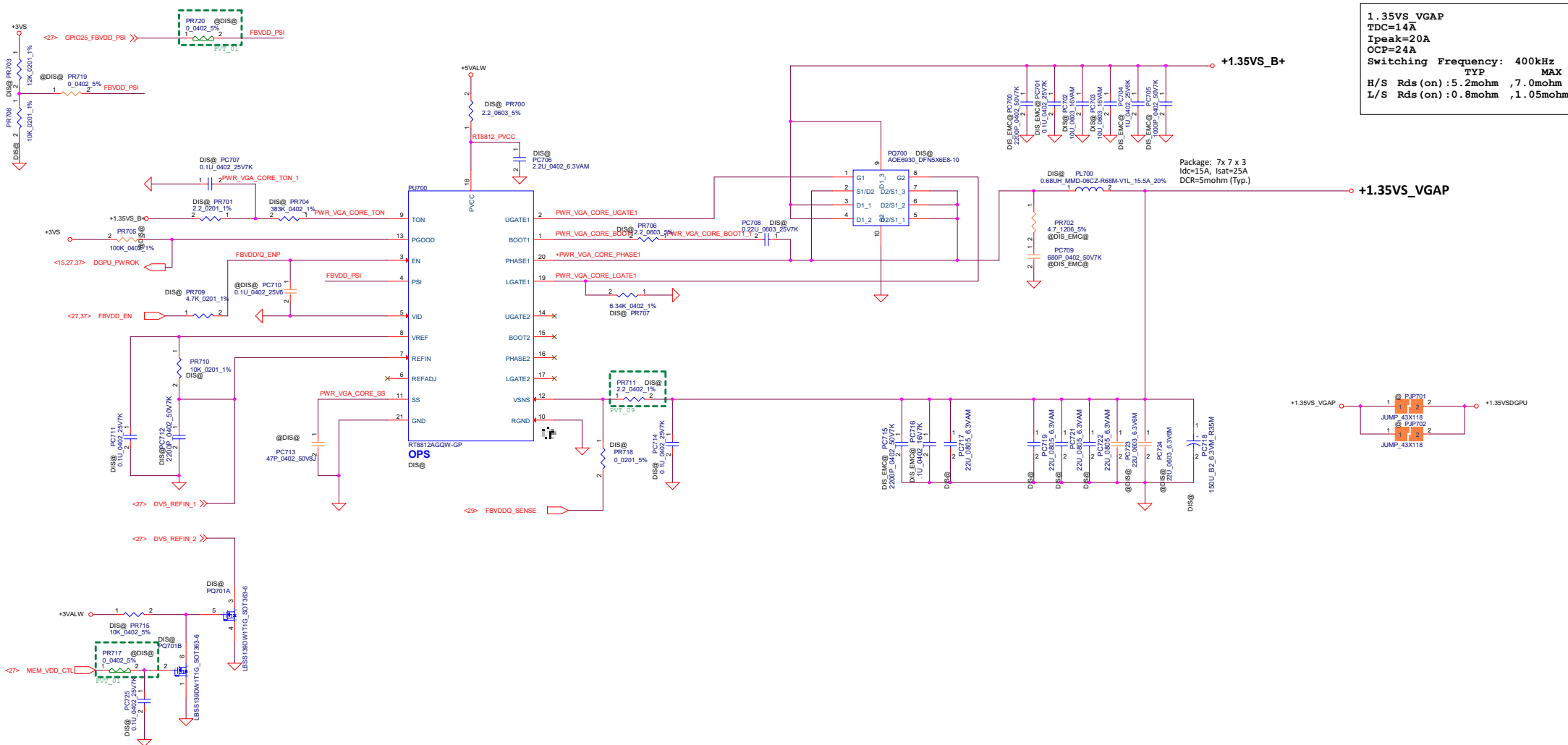
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				Sheet	94 of 100


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for dGPU SKU
@DIS@ : Nopop Component
DIS@: POP for dGPU SKU
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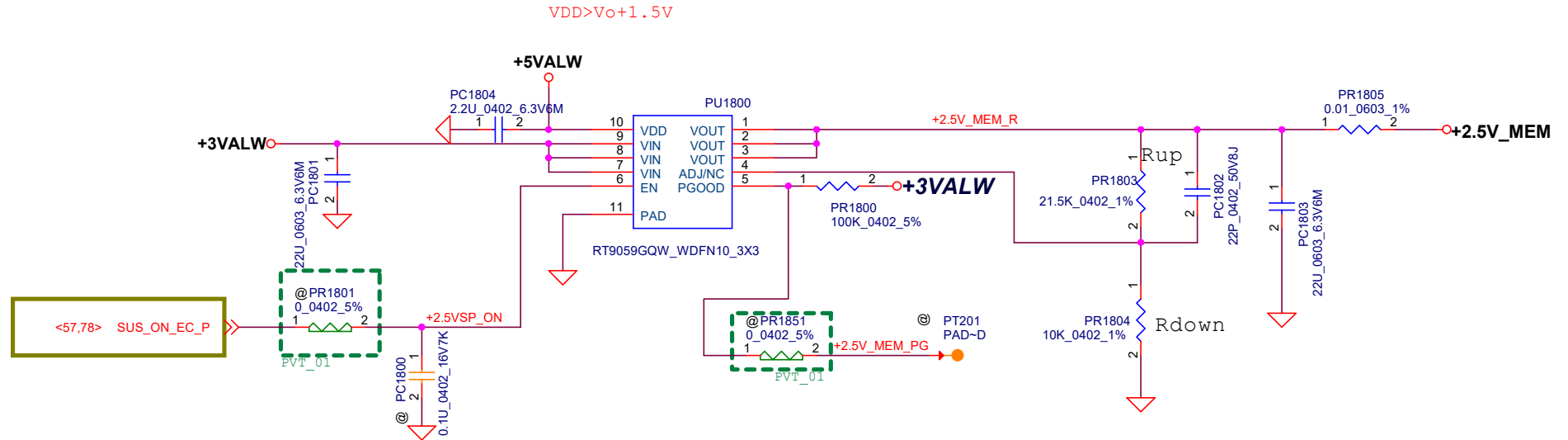


VRAM Control PWM IC(43.5), Support component(43.6)

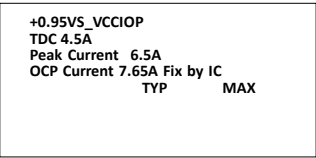
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2.5V_MEM controller(35.11), Support component(35.12)

+2.5V_MEM
TDC 1.6A
Peak Current 1.6A
OCP Current 3A



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	L*	G1	G0	YOUTP (%)
YOUTB1	0	X	X	0
	1	0	0	0.05
	1	0	1	7.878
	1	1	0	0.65
	1	1	1	2.972

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